We should first point out the difficulty in obtaining an accurate measurement of the interface state density D_{IT} on SiC. Because of the wide bandgap of SiC, deeper-lying interface states at the SiO_2/SiC interface are not in thermal equilibrium with the semiconductor at room temperature, and the occupancy of interface states cannot follow changes in the DC bias [2]. To correctly measure the interface state density using CV techniques, it is necessary to heat the sample enough that the states can remain in quasi-steady-state as the gate voltage is changed. This has not been recognized by all SiC researchers, and several erroneous reports are present in the literature. At Purdue we use a modified hi-lo capacitance technique and the AC conductance technique at elevated temperatures to characterize the SiO_2/SiC interface [3].

Purdue has recently completed the first phase of a program, sponsored by BMDO and the Semiconductor Research Corporation (SRC) to investigate and optimize the SiO_2/SiC interface. In this project, MOS capacitors are fabricated on both aluminum and boron-doped epilayers on the (0001) Si face of p^+ 6H-SiC wafers. The epilayers are doped in the range 1-2 x 10^{16} cm^{-3}. Two different pre-oxidation cleaning procedures are studied: the "Piranha" clean and the "RCA" clean. In addition, two procedures are investigated for loading wafers into the oxidation tube. In the first procedure, wafers are loaded in Ar with the tube stabilized at the oxidation temperature. In the second procedure, wafers are loaded in O_2 at 750 °C and the temperature is then raised to the final oxidation temperature. All devices in the study are oxidized at 1150 °C in wet O_2, followed by a 30 minute in-situ Ar anneal at 1150 °C. Wafers are removed from the furnace by one of two procedures. In the "fast pull" procedure, wafers are withdrawn from the furnace in about 100 seconds. In the "slow pull", the furnace temperature is gradually reduced over a period of 1 hour to about 900 °C before unloading. To complete the MOS capacitors, Al is thermally evaporated using an alumina-lined tungsten boat, and circular metal gates are defined by optical lithography and wet etching.

The preoxidation clean and load/unload procedures have a significant impact on the interface quality. Table 1 summarizes the effects of these procedures on SiC MOS capacitors with boron doped epilayers. Wafers which are Piranha cleaned and loaded and unloaded in Ar at 1150 °C have fixed charge densities in the low-10^{12} cm^{-2} range and interface state densities in the mid-$10^{11}cm^{-2}eV^{-1}$ range (line 1). These values are quite high compared to silicon interfaces. Thermal shock on the SiC/SiO_2 system caused by unloading at 1150 °C has a slight adverse effect on interfacial quality. This is seen in line 2 of Table 1, where the gentler unloading procedure reduces the fixed charge and the interface state density by about 10%. A factor-of-two reduction in both the fixed charge and the interface state density results from the use of the more comprehensive RCA clean prior to oxidation, as shown by line 3 of Table 1. As seen in line 4 of Table 1, the low-temperature loading procedure reduces the interface state density to about 1.5 x 10^{11} cm^{-2} eV^{-1} and the fixed charge density to 9 x 10^{11} cm^{-2}, the lowest values ever reported on the p-type SiC/SiO_2 interface. Figure 1 shows interface state density versus bandgap energy for lines 1, 3, and 4 of Table 1.

Cleaning Procedure	Loading Procedure	Unloading Procedure	D_{IT} x 10^{11} ($cm^{-2}eV^{-1}$)	Q_F/q x 10^{12} (cm^{-2})
1 -- Piranha	in Ar	fast	6.0	2.6
2 -- Piranha	in Ar	slow	5.4	2.3
3 -- RCA	in Ar	fast	2.4	1.4
4 -- RCA	in O_2 at 750 °C	slow	1.5	0.9

Table 1. Summary of oxidation experiments performed at Purdue. All oxidations are conducted at 1150 °C in wet O_2 followed by a 30 min. Ar anneal. Epilayers are doped with boron at 1-2 x 10^{16} cm^{-3}.

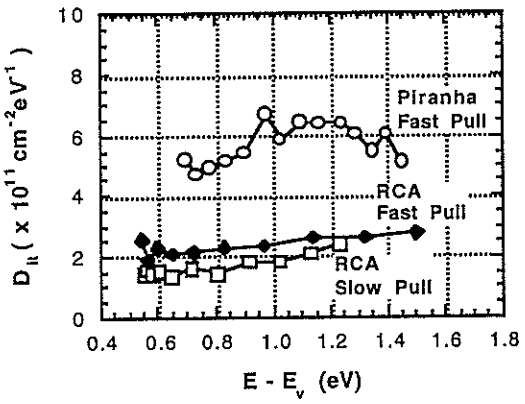


Figure 1. Comparison of D_{it} for different oxidation conditions, measured by hi-lo CV at 340 °C.

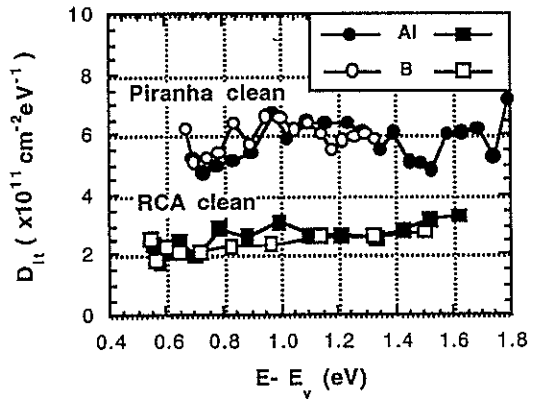


Figure 2. D_{it} of MOS capacitors on Al - and B-doped epilayers for two different oxidation conditions.

Palmour, et al. [4] have shown that during thermal oxidation of Al-doped SiC, Al atoms are incorporated into the oxide at about the same density as the dopant density in the semiconductor. This had led to speculation that the fixed charge and interface states at the SiO_2/p-type SiC interface might be due to the incorporation of Al at the interface In our study, we investigated the use of boron as an alternative p-type dopant for MOS devices. Boron is the p-type dopant used in silicon, and does not degrade the SiO_2/Si interface. The results are summarized in Fig. 2, which shows interface state density versus energy for two oxidation conditions [2]. It is seen that even though D_{it} is quite different for the two procedures, there is no significant difference in interface quality between Al- and B- doped epilayers.

(e). Thick oxides are used for field and intermediate dielectrics and as passivation layers for field termination on high-voltage devices. It is not practical to grow thick oxides by conventional thermal oxidation due to the long times and temperatures involved. Moreover, dopant redistribution (segregation) into a growing thermal oxide can be a problem. We use several techniques, depending on the circumstances: (i) deposition of thick SiO_2 by either LPCVD or PECVD, (ii) deposition of an amorphous silicon layer which is later converted to SiO_2 by thermal oxidation, or (iii) application of spin-on-glass (SOG).

(f). Ohmic and Schottky contacts. Ohmic contacts are formed to n- and p-type layers by annealed nickel and annealed aluminum, respectively. These procedures are quite routine, and specific contact resistivities in the 10^{-6} Ω-cm^2 range can be obtained to heavily-doped n-type SiC. Ohmic contacts to p-type material are more difficult, and contact resistivities range from 10^{-3} Ω-cm^2 for lightly-doped material to 10^{-5} Ω-cm^2 for heavily-doped material. Schottky contacts are easy to fabricate, and Fermi level pinning is not observed. As a result, barrier heights are a function of the metal, and a wide range of barrier heights are attainable. Typical metals used for Schottky contacts on SiC are Au, Pt, and Ti.

(g). Metal and polysilicon deposition procedures are similar to silicon, and no unusual problems are encountered. Purdue uses boat-evaporated aluminum or LPCVD polysilicon as gate materials for SiC MOSFET's. Cree uses molybdenum or polysilicon.

4.3. Status of SiC Device Development

In parallel with our work on the unit processes described above, both Purdue and Cree have maintained active programs in SiC device development. In May 1992, Purdue received a BMDO contract to develop the first SiC charge-coupled devices (CCD's) for UV image sensors.

Figure 3 shows an overlapping-gate four-phase buried-channel CCD fabricated under this program [5]. This device uses dual-level metallization to interconnect the four CCD phases. The even-numbered MOS gates are POCl-doped polysilicon, patterned by RIE and sealed by thermal oxidation. Odd-numbered gates are thermally evaporated aluminum. Input and output circuits use ion-implanted non-self-aligned n-channel MOSFET's.

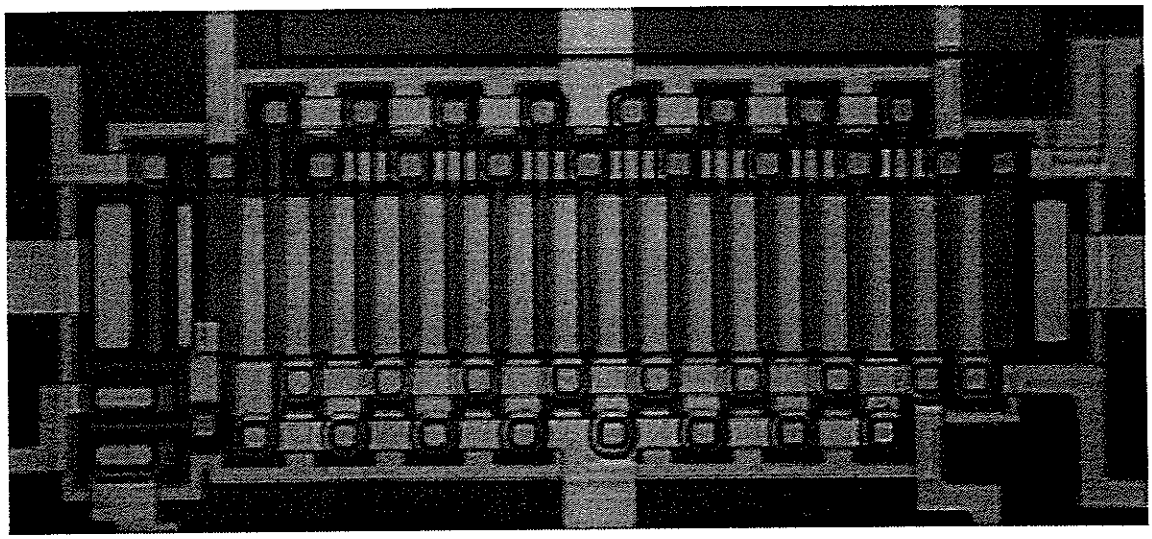


Figure 3. Photograph of a SiC overlapping-gate four-phase buried-channel CCD fabricated at Purdue.

In March 1993, Purdue and Cree were awarded $4.2M by BMDO/IST to develop a monolithic SiC 1024-bit nonvolatile RAM chip. The SiC NVRAM cell is an extension of the work conducted at Purdue in the late 1980's on one-transistor memory cells in GaAs [6]. The basic NVRAM cell [7] consists of a pn junction storage capacitor vertically integrated with an npn bipolar access transistor, as shown in Fig. 4. Charge is stored on the floating collector of the npn BJT, which is designed to have a large capacitance to the p-type substrate. The epilayers are grown at Cree, device fabrication is done at both Purdue and at Cree, and testing is performed at Purdue. The n-type emitter of the BJT is formed by ion implantation, and the structure is trench isolated by RIE. The sidewalls are passivated by thermal oxidation, and ohmic contacts are formed to the p-base and n-emitter by alloyed Al and Ni, respectively. Figure 5 shows operating waveforms of the NVRAM cell at room temperature, illustrating electrical reading and writing. For these tests, the charge state of the cell is monitored by the cell capacitance measured between the base and the substrate.

The NVRAM takes advantage of the extremely low electron-hole generation rate in SiC. Since the thermal generation rate decreases exponentially with bandgap energy, 6H-SiC (E_G = 3.0 eV) should have a thermal generation about 16 orders-of-magnitude lower than in silicon at room temperature. This means it would theoretically take *over one million years* for charge to be restored to the floating collector of the NVRAM cell at room temperature! We have studied the generation rates in the bulk semiconductor and at the passivated surfaces of pn junction storage capacitors as a function of temperature, electric field, doping density, dopant species, oxidation procedure, polytype (6H and 4H), and contact annealing procedure. By measuring capacitance recovery transients at elevated temperatures (typically 250-350 °C), we have verified that the charge recovery is thermally activated with an activation energy of half bandgap (1.5 eV), and the high temperature data does indeed extrapolate to a room temperature storage time of over 10^6 years [8]. As the result of careful studies of defect incorporation and surface passivation, we have now increased the extrapolated room temperature storage time to over 10^8 years.

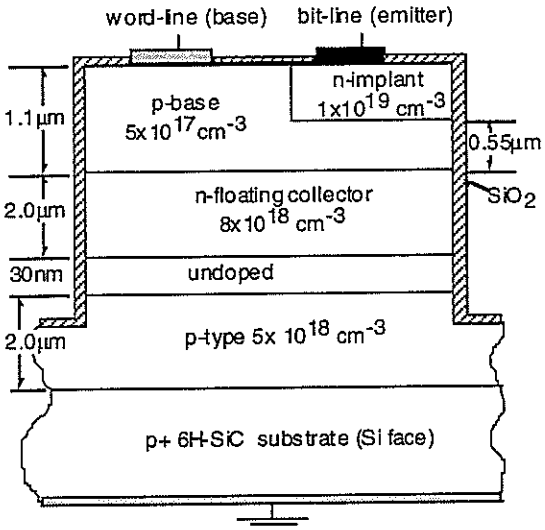


Figure 4. Cross section of the SiC vertically-integrated bipolar NVRAM cell fabricated at Purdue.

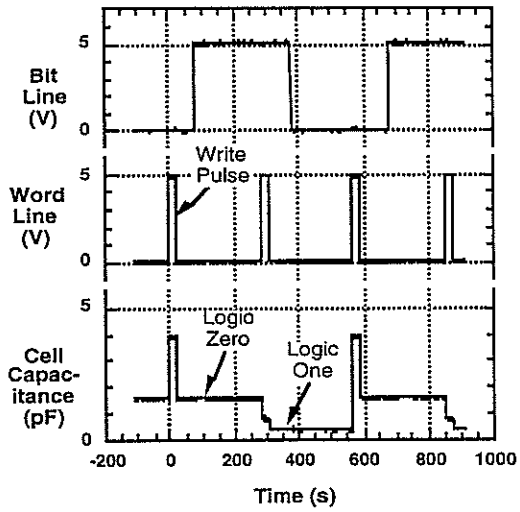
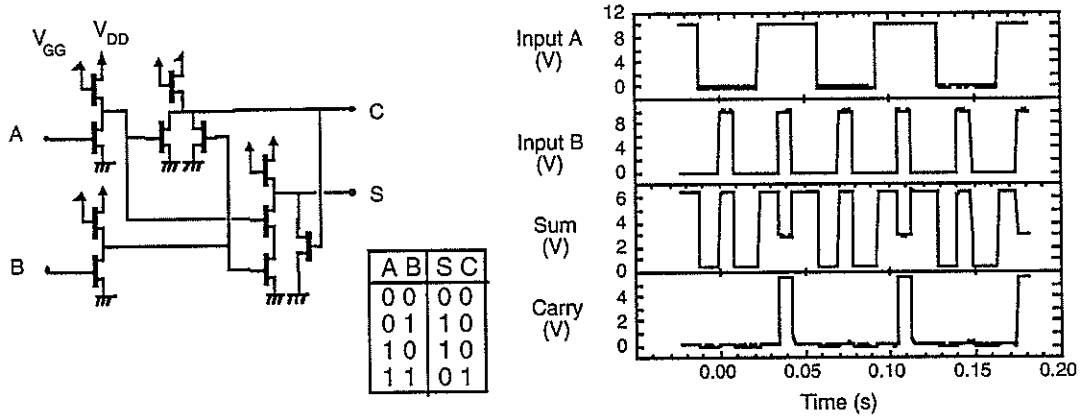


Figure 5. Operating waveforms of the SiC NVRAM cell at room temperature.



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 6. SiC NMOS half adder schematic (left), truth table (center), and room temperature waveforms (right).

In February 1994, Purdue announced the first monolithic integrated circuits in SiC [9], realized using ion-implanted aluminum-gate n-channel MOS transistors arranged in a non-saturating enhancement-load logic configuration. The circuits included inverters, NAND and NOR gates, XNOR gates, D-latches, RS flip-flops, binary counters, and half adders. All circuits were functional from room temperature to over 300 °C. Figure 6 shows the circuit diagram, truth table, and waveforms of the SiC half adder [10].

The examples cited above give an indication of Purdue's experience in SiC device development. However, this discussion does not include many of the devices demonstrated independently by Cree Research. These include SiC LED's, UV photodiodes, the first SiC microwave MESFET's, and the first SiC MOSFET's (both enhancement and depletion mode). Cree also demonstrated the first SiC high voltage rectifiers (having the highest current ratings yet reported), the first SiC thyristors, and the first (and only) vertical power MOSFET's in SiC [11].

5. Issues in Developing Power Devices in SiC

Because of the unique properties of SiC, power devices in SiC will in some ways be very different from similar devices in silicon, and a simple translation of silicon concepts to SiC will not always be possible. The main advantage of SiC is its breakdown field, which is about 8x higher than in silicon. However, the hole and electron mobilities are a factor of 2 – 5 lower than in silicon, and the electron mobility in 6H-SiC is highly anisotropic. Minority carrier lifetimes in SiC are about 1000x shorter than in silicon. In spite of recent progress, the SiO_2/p-type SiC MOS interface still exhibits interface state and fixed charge densities about a factor of 3 higher than silicon. Since the crystal lattice is not isotropic, MOS interfaces formed on vertical sidewalls (as in UMOSFET's) may have electrical properties inferior to those on the Si-face.

Bipolar power devices such as the insulated gate bipolar transistor (IGBT) and the MOS-controlled thyristor (MCT) are widely used in silicon. The IGBT provides a high blocking voltage and a low specific on-resistance, but it is restricted to low-frequency applications because of its slow switching speed. In SiC, an IGBT would exhibit higher blocking voltages and/or much lower on-resistances than a comparable silicon device, and it would be very fast, owing to the much shorter minority carrier lifetimes. However, the short lifetimes also result in very low current gains, typically in the range of 10 – 12. This means that SiC bipolar devices would require very large base currents, on the order of 10% of the on-state current of the device. To remedy this situation, one goal of this MURI program will be to increase the minority carrier lifetimes in SiC. We will do this by identifying the dominant recombination-generation (RG) centers in SiC epilayers and modifying growth procedures to reduce the RG center density.

Silicon power MOSFET's are not practical for high-voltage (>1000V), high-current applications because of their relatively high on-resistance, which arises primarily from the drain drift region. In SiC, the drift region resistance can be 100 – 200x smaller than in a comparable silicon device, making high-voltage SiC power MOSFET's very attractive. For drain voltages less than about 1000 V, however, the on-resistance of a SiC MOSFET is actually dominated by the channel resistance. We believe the MOSFET channel resistance can be reduced by as much as a factor of 4 – 5 by optimizing the SiC MOS interface, thereby reducing the fixed charge density and the associated Coulomb scattering.

The typical power MOSFET in silicon is a DMOS (or doubly-diffused MOS) structure, as illustrated in Fig. 7. The short channel length is achieved by diffusing the p-type base layer and the n+ source through the same oxide window, thus removing any dependence on alignment of photomasks. The p-type base must have a sufficient number of dopant atoms per unit area (thickness times concentration) to prevent punch-through by the drain electric field in the blocking state. Unfortunately, this device concept is difficult to translate to SiC because it is not feasible to thermally diffuse dopant atoms in SiC. One might artificially construct a similar structure using ion implantation, but the channel length would then be defined by a mask alignment, and it would be difficult to implant the p-type impurity to sufficient depth to prevent punch-through. For these reasons, a vertical UMOSFET structure is the most practical in SiC. Because of its importance, we will analyze the UMOSFET device next.

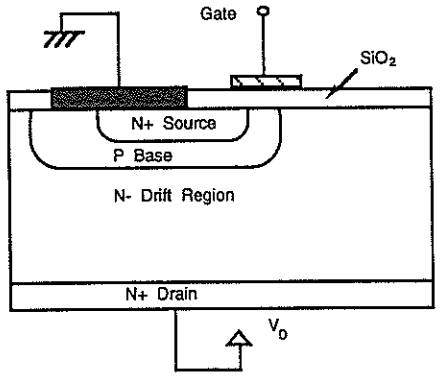


Figure 7. Cross section of a typical silicon DMOSFET. The p-type base is diffused through the same oxide mask as the n+ source. Such a procedure is not practical in SiC, owing to the inability to thermally diffuse dopants at reasonable temperatures.

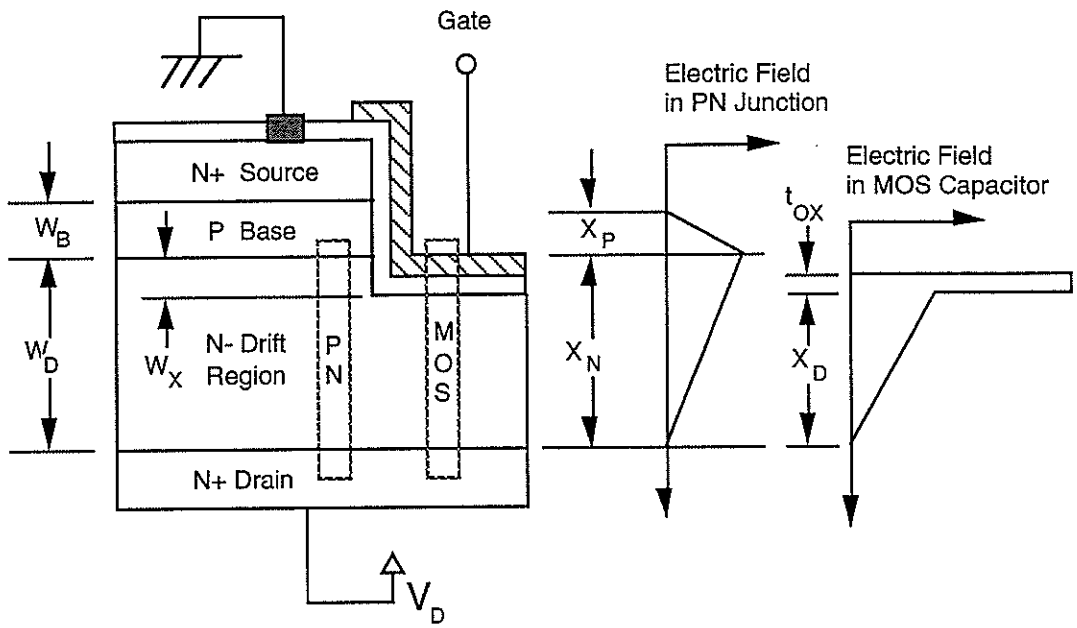


Figure 8. Cross section of UMOS transistor. On the right are plots of the electric field in the dashed portions of the device: the pn junction between the p-base and the drain, and the MOS capacitor under the etched trench. The fields are higher under the trench, and the highest field occurs in the oxide.

To analyze the UMOSFET, we shall use the idealized geometry of Fig. 8. The trench extends below the p-base region by a distance W_X. We will analyze the electrostatics in two regions: the boxed region labeled "PN", and the boxed region labeled "MOS". The breakdown field of 6H-SiC depends on the doping in the lightly doped region according to

$$E_{BR} = 19500\,(N_D)^{0.131} \text{ [V/cm]} \tag{1}$$

The electric field in the pn junction is shown on the right side of Fig. 8. The maximum field occurs at the pn junction, and the depletion widths X_N and X_P are given by

$$X_N = \frac{\varepsilon_S E_{BR}}{q N_D} \quad \text{and} \quad X_P = \frac{\varepsilon_S E_{BR}}{q N_A} \tag{2}$$

where N_A is the doping of the p-type base region. The maximum voltage which the junction can sustain is the integral of the electric field, and is given by

$$V_{MAX} = \frac{q N_D X_N^2}{2\,\varepsilon_S} + \frac{q N_A X_P^2}{2\,\varepsilon_S} \tag{3}$$

Thus, for each possible choice of drift region doping N_D and base region doping N_A, we can calculate E_{BR} using (1), X_N and X_P using (2), and V_{MAX} using (3).

The region under the trench forms an MOS capacitor. When the UMOSFET is turned off, the gate will be at ground potential, the drain (substrate) will be at the maximum drain voltage, and the n- drift region will be fully depleted. The peak electric field in the MOS capacitor will be larger than in the pn junction. The maximum voltage across this part of the structure will be limited by avalanche breakdown in the semiconductor or by oxide breakdown, whichever comes first. The avalanche breakdown field is given by (1). We have measured the oxide breakdown field E_{BOX} on SiC to be around 9 MV/cm. To minimize charge injection into

the oxide, which leads to early device failure, we will limit the oxide field to 3 MV/cm in this design example. Note that the field in the oxide is higher than the peak field in the semiconductor due to the difference in dielectric constants. The field is also increased by the positive fixed charge Q_F at the interface. From Table 1, Q_F/q is typically about 10^{12} cm^{-2}.

In the MOS portion of the structure, we require that the peak field in the semiconductor at the interface be the smaller of: (a) the breakdown field given by eqn. (1), or (b) the semiconductor field when the oxide field is equal to E_{BOX}. Thus,

$$E_S = \mathrm{Min}\begin{cases} E_{BR}(N_D) \\ \dfrac{\varepsilon_{OX} E_{BOX} - Q_F}{\varepsilon_S} \end{cases} \tag{4}$$

The depletion depth under the MOS gate $X_D = \varepsilon_S E_S / (q N_D)$, and the maximum gate-to-substrate voltage is given by

$$V_{G\text{-}D,MAX} = \frac{q N_D X_D^2}{2 \varepsilon_S} + \frac{t_{OX}}{\varepsilon_{OX}} \left(Q_F + q N_D X_D \right) \tag{5}$$

where t_{OX} is the oxide thickness and ε_{OX} is the oxide dielectric constant. For the calculations which follow, the base region doping N_A is chosen to be 10^{17} cm^{-3} for drain dopings $N_D < 10^{17}$ cm^{-3}, and N_A is set equal to N_D for $N_D > 10^{17}$ cm^{-3}. This minimizes the increase in X_P, which would lead to a longer channel length W_B and higher channel resistance in the on-condition. Oxide thickness is assumed to be 50 nm. Figure 9 shows the breakdown voltage for the UMOSFET as calculated using (3) for the pn junction and (5) for the MOS region under the trench. The upper curve is similar to that quoted for the maximum voltage of the UMOSFET by Bhatnagar, Alok, and Baliga [12], but the true breakdown voltage is limited to much lower values by the MOS region under the trench. This effect is ignored in the theoretical analysis by Baliga, with the result that **the breakdown voltage is overestimated by a factor of six to ten.** In a real device, the breakdown voltage will be even lower, since the electric field at the trench corner is about a factor of two higher than under the bottom of the trench. Figure 10 shows the critical design dimensions (defined in Fig. 8) as calculated using equations (1) – (5). These figures can be used to design a SiC UMOSFET to withstand blocking voltages up to several thousand volts.

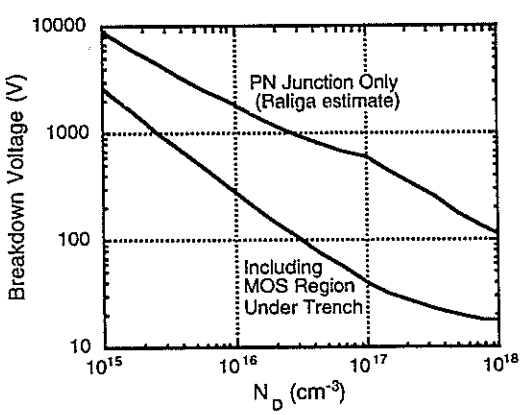


Figure 9. Breakdown voltage of SiC UMOSFET's as a function of drift region doping. The maximum voltage is limited by the MOS region under the trench.

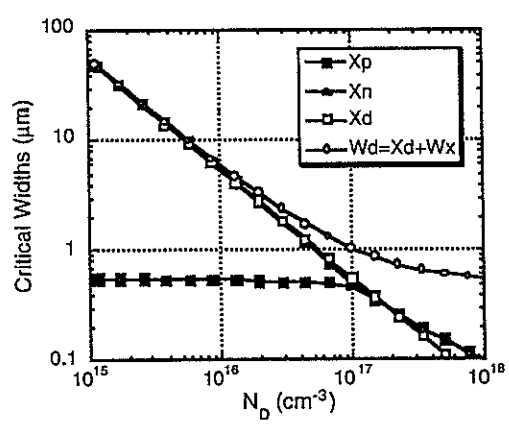


Figure 10. Critical design dimensions of the UMOSFET as a function of drift region doping.

Our analysis of the UMOSFET indicates that the maximum voltage will be limited by oxide breakdown in the trench region. This is a significant problem which was ignored in Baliga's analysis. We plan to follow two approaches to alleviate this problem. In the first approach, the UMOSFET geometry of Fig. 8 will be modified to include a p-type field suppression layer implanted in the region at the bottom of the trench. This p-type layer will be completely depleted under the blocking condition, resulting in a reduction in the electric field near the surface. In the second approach, we will eliminate the trench entirely and investigate the use of MeV ion implantation to fabricate a planar DMOS-like MOSFET, as shown in Fig. 7.

Cree Research has fabricated the first power UMOSFET's in SiC, using both the 6H and 4H polytypes [11]. The highest blocking voltage achieved to date is 180 V and the highest current density is 550 A/cm^2, both observed on the 4H polytype. The limit to higher voltage in these devices is oxide breakdown at the bottom of the trench, as predicted in our analysis. The electron surface mobility in the MOSFET channel along the a-axis face of the sidewall ranges from 7 – 20 cm^2/Vs, considerably lower than the 40 – 50 cm^2/Vs typically seen on the silicon face. The saturated drain current increases with temperature to around 300 °C, where the devices begin to experience gate oxide failure. This indicates more research is needed on oxide reliability, especially on the sidewall oxides.

The MOS channel of the UMOSFET is formed on etched sidewalls of the trench. Since the SiC crystal lattice is not isotropic, surfaces other than the (0001) Si-face have approximately equal numbers of silicon and carbon atoms exposed, and these surfaces are expected to have electrical properties inferior to the (0001) Si-face. Purdue and Cree are collaborating on the first studies of the SiO_2/SiC interface on the $(1\bar{1}00)$ and $(11\bar{2}0)$ a-axis surfaces of 6H-SiC. Preliminary results [13] suggest that interface state and fixed charge densities on the vertical sidewalls are about an order-of-magnitude higher than on the Si-face (Figs. 1 and 2). This explains why the channel mobilities in Cree's UMOSFET's are significantly lower than in MOSFET's on the Si-face. These lower mobilities are critical, because the specific on-resistance in these devices is dominated by the MOSFET channel rather than by the drift region. Clearly, more research is needed to improve the MOS properties of the sidewalls.

6. Status of III-V Nitride Material Technology

6.1 III-V Nitride Epitaxy by MOCVD

Recently, Dupuis and co-workers at UT-Austin reported the growth of heteroepitaxial GaN films by low-pressure metalorganic chemical vapor deposition (MOCVD) on (0001) sapphire substrates having an X-ray rocking curve full-width at half maximum (FWHM) of less than 40 arc sec.[14] To our knowledge, this is the best reported value for any III-V nitride epilayer grown on sapphire. We have also reported the observation of Pendellösung fringes in the X-ray rocking curve for high-quality GaN films.[15,16] Optical transmission data taken at 300K confirm that the films have a direct energy gap at E_g ~3.4 eV. Room-temperature photoluminescence (PL) studies and electrical measurements have further established the quality of these films. The structural quality of the GaN epitaxial films is analyzed using a Blake Instruments high-resolution five-crystal diffractometer and computer-controlled measurement electronics using custom software. Cu K_α radiation is used and rocking curves through the (0002) GaN and sapphire lattice Bragg peaks are made to analyze the quality of the films. The FWHM of the (0002) GaN diffraction peak has been studied as a function of the thickness of the GaN film. The FWHM of the ~0.3 μm-thick films are ~100 arc sec while thicker films (~0.7 μm) have reproducible FWHM values $\Delta\Theta$~38 arc sec. TEM analysis of these layers has confirmed the high quality of the GaN material and the GaN/sapphire interface.[17] For comparison, the FWHM of the X-ray rocking curve for GaN/sapphire films reported by other workers includes a best result of $\Delta\Theta$~96 arc sec for a GaN heteroepitaxial film having a

thickness ~4 μm grown by MOCVD on a GaN buffer layer, while a more typical "best" FWHM is $\Delta\Theta$~360 arc sec or more for ~4 μm-thick films. **Our FWHM values represent a significant improvement in the quality of heteroepitaxial III-V nitride films.**

In addition to the nitride-related work, Dupuis' group has been investigating various device and materials issues in the related As- and P-containing III-V quaternary systems. We have recently succeeded in the MOCVD growth and the fabrication of InGaAsP-InP heterojunction bipolar transistors (HBT's), p-i-n and light-emitting diodes (LED's), and injection lasers. Also, we have grown novel AlGaAs-GaAs [18], and InAlP-InGaP [19] quantum-well (QW) heterostructures for optoelectronic device applications. Many of the broad range of materials and device issues that are being addressed in Dupuis' group are highly parallel to the issue of nitride-based high-power devices and it is expected that much of our experience can be applied directly to the proposed high-power device research program.

6.2 III-V Nitride Epitaxy by MBE

Prof. Streetman's group at UT-Austin has recently demonstrated the growth of GaN films using an novel N_2 cracker. Using this N source and a standard Ga metal effusion cell, we have grown GaN on sapphire substrates with growth rates approaching those of standard III-V MBE (about 0.6 μm/hr). This is an important breakthrough, since MBE growth of GaN using standard ECR sources of N has resulted in growth rates ~0.2 μm/hr.

6.3 III-V Arsenides and Phosphides by MBE

J. M. Woodall has a world class MBE facility at Purdue for the MBE growth of the III-V arsenides and phosphides. Our effort includes high speed electronic and photonic devices including high speed 1.3-1.5 μm detectors and visible LEDs using non-lattice-matched InGaP on GaP substrates. Prof. Woodall's group at Purdue has recently demonstrated the growth of p-type GaAs with greatly reduced surface state densities. This reduced density is maintained even after exposure to air. This result could form a basis for building high power MOSFET switching device structures using GaAs and possibly GaInP, a material which has a figure of merit nearly 20x that of silicon for power switching applications.

In addition, Prof. Woodall is one of the leading experts on the doping of compound semiconductors and the formation of contacts to compound semiconductors. He has invented and developed numerous contact structures, and his work has lead to the ability to achieve higher doping levels than previous state-of-the-art values, particularly in GaAs. His theoretical work led to the MBE growth condition used to achieve p-type doping of ZnSe.

7. Research Plan

7.1 Objectives

The objective of this project is to develop the technology for power switching devices in the wide bandgap semiconductor SiC and/or the III-V nitrides and to transfer this technology into commercial production.

7.2 Approach

We believe that SiC offers the most direct path to manufacturable power switching devices. The III-V nitrides are promising materials based on their electronic properties and on encouraging advances in the last two years, but more basic research is needed before the nitrides will be ready for commercial production of devices. We plan to focus on SiC device

development in the first three years of the MURI program, and to begin device development in the III-V nitrides during the third or fourth year, depending on progress in the materials research.

Our program is structured to take SiC and/or III-V nitride devices from research to development to commercial production. This path is provided by the participation of Cree Research. Cree is the world leader in SiC materials research, and is the only commercial source of SiC wafers. Cree also has manufacturing and marketing experience, having sold over 10 million SiC blue LED's. Cree has made a corporate decision to develop and market SiC (and/or III-V nitride) power devices as commercial products, and is actively developing power device technology using internal and external funds. Cree's participation in this MURI program therefore provides a direct path to move the technology from research and development into commercial production.

Cree and Purdue have a long history of successful collaboration. We began working together in 1990, and in March 1993 we were awarded a $4.2M contract from BMDO/ONR to develop nonvolatile RAM's in SiC. Purdue has been independently conducting research on SiC power devices since winning the SRC's power device initiative in 1993. Cree has even more experience, having developed SiC and MOS bipolar transistors, high-voltage rectifiers, thyristors, and power UMOSFET's. In the MURI program, we will build on our SiC device experience and our history of collaboration to jointly develop the technology for power devices in SiC, and Cree will then transition these results into manufacture.

While SiC device development is the core of our proposal, we will also conduct an aggressive research program on III-V nitride semiconductors, led by R. D. Dupuis and B. G. Streetman at UT-Austin. Dupuis will pursue MOCVD growth, while Streetman will concentrate on MBE. M. R. Melloch and J. M. Woodall of Purdue and M. G. Spencer of Howard University will investigate the growth of heterojunctions between SiC and the III-V nitrides. In addition, Spencer will explore wide-area growth of 3C-SiC on silicon wafers using compliant substrate techniques. If successful, these SiC-on-Si wafers could serve as substrates for subsequent growth of III-V nitrides. At Purdue, Woodall and Melloch will study new ohmic and Schottky metallurgy for the III-V nitrides and investigate other III-V materials (e.g. InGaP and low-temperature-grown GaAs) as alternative materials for power devices.

The III-V nitride activity will be reinforced by the participation of Cree Research. Cree is developing GaN blue LED's for commercial manufacture, and is now growing both n- and p-type GaN over a wide range of doping from nearly intrinsic to nearly degenerate. Cree will act as a *third* source of III-V nitride epilayers and heterojunctions for this project (along with Dupuis' MOCVD and Streetman's MBE), and if the nitride device development is successful, Cree will manufacture and market III-V nitride power devices grown on SiC substrates.

7.3 Development of Power Device Technology in SiC

7.3.1 SiC Crystal Growth and Materials Improvement

The first major challenge is to improve the SiC crystal growth technology. The improvements need to take two forms: increased wafer size, and reduced defect and impurity density. Cree presently sells 1.188" diameter SiC wafers in both 4H and 6H polytypes, and produces 2" diameter wafers of both polytypes for internal production. Cree expects to begin selling 2" wafers commercially soon and to be producing 4" wafers by 1999. However, problems arise when one attempts to insert the current 2" SiC wafers into existing silicon production lines. The oldest silicon lines handle 4" wafers and the newer lines handle 6" or 8" wafers, and none of the automated processing equipment will work with the smaller SiC wafers. Although this is not a materials science issue, it remains a significant practical problem. We will propose innovative solutions to this problem in the next two sections.

Defects in current SiC wafers include micropipes, line defects, and electrically active impurities. Micropipes are tubes, up to tens of microns in diameter, which penetrate the wafer and propagate into subsequent epilayers. Micropipes have been shown to correlate directly with premature breakdown in reverse-biased pn junctions [20]. Cree has made substantial progress in

reducing micropipe density ($D_0 \approx 27$ cm^{-2} have been recently achieved), and expects these defects will be essentially eliminated within the next 3 – 5 years. A larger number of line defects are visible as etch pits, but they do not seem to affect the yield of power devices.

Electrically active defects and impurities in the material serve as recombination-generation centers, and are responsible for the short minority carrier lifetimes in SiC. As part of the BMDO-sponsored nonvolatile RAM program, Purdue and Cree have obtained statistical data linking generation rate in pn junctions to epitaxy and processing conditions. Under the MURI program, we will expand this study to identify specific defect levels using deep level transient spectroscopy (DLTS).

Cree Research will soon receive an ARPA contract for a $6.9M program to address the SiC crystal growth issues, both from a standpoint of increasing wafer size and reducing defect density. Research conducted at Cree under the ARPA contract will directly benefit this research program. **Aligning the MURI program on power switching devices with the ARPA program on SiC materials improvement makes good sense.** We will maintain a close collaboration between the crystal growth activities at Cree and the device development activities of this MURI program.

7.3.2 Wide-Area Growth of SiC on Silicon

One innovative approach to achieving large-area SiC substrates for power device fabrication is the growth of SiC on silicon. Michael G. Spencer of Howard University will investigate a silicon-oxide-silicon compliant substrate technique to improve the quality of SiC films grown on silicon by CVD. Dr. Spencer has over eight years experience in the growth of SiC by both bulk and sublimation techniques, and the Material Science Research Center at Howard University includes an epitaxial reactor which is ideally suited for this work. The unit has two chambers, one dedicated to III/V nitrides and alloys and the other to SiC. The chambers are vacuum interlocked, and samples can have either films of nitrides or carbides grown without the material seeing ambient. The system also features a RHEED gun for in-situ analysis.

Silicon wafers have previously been investigated as substrates for several lattice-mismatched systems, including GaAs/Si, GaP/Si, Ge/Si and SiGe/Si. In systems where the lattice mismatch is small (i.e. less than 1%), conditions can usually be found for two-dimensional growth, and films of good quality can be obtained until the pseudomorphic limit is reached. When films grow pseudomorphically, the epilayer deforms in the plane perpendicular to the growth direction in order to accommodate the lattice constant of the substrate. The pseudomorphic thickness limit is reached when stress in the crystal due to the deformation causes the epilayer to relax by forming misfit dislocations. The pseudomorphic thickness limit is a function of the lattice mismatch – for InAs on GaAs (7% mismatch) the limit is about one monolayer, while for $In_{0.2}Ga_{0.8}As$ on GaAs the limit is about 100 Å. In SiC on silicon, where the lattice mismatch is > 20%, the pseudomorphic limit is less than one monolayer. However, the most destructive defects found in films of SiC grown on Si are not dislocations but rather stacking faults. Stacking faults similar to those seen in the SiC/Si system are also seen in the GaP/Si and GaAs/Si systems. The fact that stacking faults are observed in these other systems where the lattice mismatch is significantly less supports the view that stacking fault generation is not directly connected to lattice mismatch, but rather is related to nucleation problems [21,22].

The growth of SiC on silicon is a two-step process consisting of a carbonization layer followed by a growth layer [23-37]. The carbonization layer is formed by exposing the silicon to a stream of carbon species (usually propane) at a high temperature. Optimization of this process results in the surface conversion of the silicon to SiC with a conversion depth of 100-300 Å. Growth of SiC is usually produced by adding a silicon species to the gas flow (typically silane). To date, SiC-on-silicon exhibit high electron mobility (best reported value ≈780 cm^2/V-sec), but pn junctions exhibit soft breakdown at about 10 V.

We propose to utilize silicon/oxide/silicon (SOS) compliant substrates to improve the quality of SiC films grown on silicon. This compliant substrate is formed by bonding high

quality silicon to a previously oxidized silicon substrate. After bonding, the top silicon is thinned, leaving the silicon substrate, an amorphous oxide layer, and a high quality thin top layer of silicon. Substrates produced in this way have been used in research of SiGe grown on silicon. In our case, we will thin the topmost silicon layer so that it can be fully carbonized. During growth and subsequent cool-down of the film, the amorphous oxide layer will accommodate any stress due to lattice mismatch, leaving the SiC film "stress free". This technique has two potential benefits: (1) stress due to lattice mismatch will be reduced, thereby reducing misfit dislocations and increasing the pseudomorphic limit, and (2) the surface energy of the substrate will be significantly changed during the SiC growth phase, hopefully making possible a growth window in which reduction or elimination of the stacking faults will be possible. Success in growing SiC-on-silicon will also open the way for subsequent growth of GaN on SiC, which will allow for the production of high quality cubic GaN for power device applications.

Specific tasks for this section are: (1) to investigate and optimize the growth of 3C-SiC using compliant substrates, (2) to characterize the quality of these films as compared to those produced on silicon substrates, and (3) to use the 3C-SiC epilayers as a base for the growth of high quality cubic GaN.

7.3.3 Substrate Bonding

A second innovative approach to achieving large-area substrates for SiC device fabrication is the concept of *substrate bonding*. In substrate bonding, one or more SiC wafers are oxide-bonded to a larger silicon wafer, and the composite wafer is processed using existing silicon production equipment. To investigate this concept, Purdue will collaborate with Delco Electronics, Kokomo, IN. Delco operates one of the largest silicon production facilities in the United States, with over 100,000 square feet of cleanroom space producing over one million integrated circuits per day. We will interact with Delco's power device group headed by Dr. James M. Himelick. The feasibility study will proceed along two paths. One student at Purdue will investigate the technology for oxide bonding of SiC to silicon. A second student will study production equipment used in the Delco facility to identify problems which may arise, including wafer thickness, planarity, and stress. These preliminary studies will identify areas for further development. The students will be jointly supervised by Profs. Melloch and Cooper at Purdue and by Dr. Himelick at Delco.

7.3.4 Adaptive Manufacturing

The defect density in SiC epilayers is decreasing rapidly, but defects may still limit the size of power devices which can be realized under this program. If this proves to be the case, we will explore the concept of *adaptive manufacturing*.

It is common practice to design large-area power devices in terms of unit cells. Each cell contains an active device and all necessary contacts, and the cells are abutted to each other until the composite device has sufficient area to carry the desired current. In adaptive manufacturing, the device is made larger than necessary, and cells (or groups of cells) are individually probe tested after contact formation but before interconnect metallization. Using a wafer map generated by the test program, contact vias are selectively opened in the passivation layer so that the final metallization only contacts good cells. The "programming" of the via openings is done by direct wafer exposure at the photolithography step under computer control, and a photomask is not generated for this step. The devices are then sorted according to current capability and sold. As an example, Fig. 11 shows an array of SiC thyristor structures fabricated at Purdue. Using adaptive manufacturing, cells such as these can be selectively interconnected to form a large-area power device with *essentially 100 % yield*, even in the presence of material defects. In the MURI program, the concept of adaptive manufacturing will be investigated as a "fall back" procedure if the yields on large-area SiC power devices are not satisfactory.

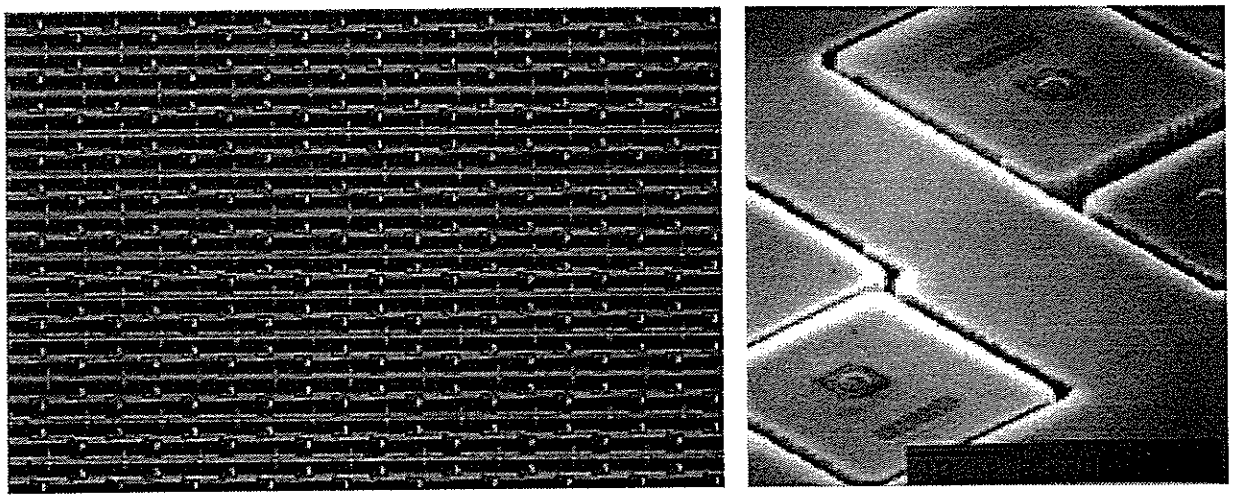


Figure 11. Monolithic array of SiC thyristor structures fabricated at Purdue under the BMDO/ONR NVRAM program (left) and SEM image of individual cells (right). Cells such as these can be selectively interconnected to form a large-area power device with essentially 100 % yield, even in the presence of material defects.

7.3.5 Optimization of the SiO_2-SiC MOS Interface

A major challenge to SiC device development is to obtain stable, repeatable, high-quality MOS interfaces on both the silicon face and the a-axis faces of SiC. As described in Section 4.2, Purdue has established a leadership position in MOS analysis of SiC. We use three techniques to characterize the SiO_2/SiC interface: a room temperature photo-CV technique, a modified high-temperature hi-lo CV technique, and a high-temperature AC conductance technique. All three techniques give consistent results for interface state density. Our MOS studies of Al- and B-doped epilayers of 6H-SiC have shown that the presence of aluminum as a dopant does not affect the interface, contrary to general expectations. We have optimized the oxidation conditions for 6H-SiC, obtaining interface state densities a factor of three lower than the best values reported by any other group. We are now conducting a study of the MOS interface on a-axis sidewalls of 6H-SiC [13], surfaces which are vital in the fabrication of power UMOSFET's. In the MURI program we will extend the current state of knowledge by conducting the following investigations:

- an investigation of post-oxidation hydrogen anneals to reduce interface state density to levels comparable to silicon
- determination of the optimum oxidation conditions for 4H-SiC (The 4H polytype is attractive for power devices because of its high electron mobility.)
- continued study and optimization of oxides on the a-axis sidewalls for power UMOSFET's
- a study of the long-term reliability of oxides on SiC at high electric fields

To create a viable SiC device technology, it is essential that the issue of reliability be addressed. Oxide reliability has been studied extensively in silicon, but so far there have been no comparable studies on SiC. Purdue and Cree have independently begun investigations into oxide reliability on SiC as a function of temperature and electric field. Under the MURI program these activities will be expanded to include the reliability of oxides on the a-axis sidewalls and etched trenches of UMOSFET's. We will study time-dependent-dielectric-breakdown (TDDB) under high-field and high-temperature stressing, and investigate the effect of processing modifications (such as nitridization) on oxide reliability and dielectric strength.

7.4 Development of Power Device Technology in the III-V Nitrides

The research to be performed in this portion of the program has four interconnected and coordinated objectives encompassing materials growth and device processing technologies:

Objective 1: To explore and develop MOCVD and MBE technologies for the growth of InAlGaN thin films and heterostructures
Objective 2: To study the carrier transport and fundamental physical properties of epilayers and heterostructures in this material system, including energy bandgap and band offsets at heterojunctions
Objective 3: To study the effects of lattice mismatch, strain, and buffer layer structures on epilayers on mismatched and lattice-matched substrates
Objective 4: To develop processing techniques for high-performance devices, including sawing, etching, Schottky barrier formation, and ohmic contacts

The III-V nitride materials in this program will be grown primarily at UT-Austin. The UT-Austin research groups headed by R. D. Dupuis (MOCVD) and B. G. Streetman (MBE) have extensive experience in the growth of III-V compound semiconductors by these techniques. UT-Austin currently has one advanced commercial multi-wafer MOCVD system growing InAlGaN films, and a second commercial MOCVD system for nitride growth was delivered in February, 1995. The MBE nitride growth will be performed in a custom-built system that employs a UT-designed plasma-assisted N_2 cracker cell installed on an EPI Gen II growth chamber. The materials and device structures will be characterized by a variety of techniques, including low-temperature and 300K photoluminescence (PL), variable-temperature Hall measurements, high-resolution X-ray diffraction (XRD), high-resolution transmission electron microscopy (TEM), scanning electron microscopy (SEM), and atomic force microscopy (AFM). All of these techniques are well-developed at UT-Austin. In addition, secondary-ion mass spectrometry (SIMS) studies will be performed on selected samples.

Cree Research is independently developing III-V nitride technology in support of its blue LED production. Cree is now growing GaN on SiC substrates with both n- and p-type dopings from nearly intrinsic to nearly degenerate. Cree will supply III-V nitride epilayers and heterojunctions for evaluation and device development in this project. As a result, our MURI program will have access to III-V nitride material from three independent sources.

7.4.1 MOCVD of III-V Nitrides

The low-pressure MOCVD growth at UT-Austin will be carried out in Dupuis' group primarily using a new production-capable multiple-wafer Emcore ES 125 advanced epitaxy system devoted specifically to growth of the III-V nitrides. In addition, Dupuis has an existing Emcore GS 3200 system that has been modified at UT for the growth of III-V nitrides. The new Emcore MOCVD system will be operational before the program begins, thus providing extensive growth capabilities for these materials. The proposed research program will utilize the low-pressure MOCVD materials technology for the growth of heteroepitaxial III-V nitride films and device structures. As discussed in Section 6.1, we have already initiated studies of the growth of III-V nitrides in the existing reactor and have reported the deposition of high-quality heteroepitaxial GaN on sapphire substrates by MOCVD. To date, MOCVD has produced the highest quality GaN films and device structures. In addition, it is extremely significant for this program that MOCVD is currently in use by Nichia Chemical Company (Japan) for the commercial production of blue- and blue-green-emitting LED's.

The MOCVD materials technology was first shown to be capable of producing state-of-the-art device-quality epitaxial compound semiconductor materials in 1977.[24,25] Since that time, MOCVD has been studied extensively and has been used to produce a wide variety of important III-V, II-VI, IV-VI and II-IV-V compound semiconductors, including the wide-bandgap (~2.0 eV) AlGaInP-GaInP materials. In fact, the MOCVD process is today in world-

wide use for the commercial production of compound semiconductor optoelectronic and electronic devices. In the MOCVD growth of conventional III-V compound heterostructures, the temperatures employed are in the 600-850 °C range. However, the growth temperatures normally used in the MOCVD growth of the wide-bandgap semiconductors AlN and GaN are in the 1050-1200 °C range.[26-34] These high growth temperatures are primarily required due to the high thermal stability of ammonia (NH_3) which is commonly used as the source of N. It is speculated that such high growth temperatures cause problems with the incorporation of a high concentration of N vacancies, as well as enhanced impurity diffusion and difficulties in the formation of abrupt heterojunctions, particularly for quantum-well and thin-layer structures. In spite of these predicted problems, the use of high V/III ratios (~2000) for the MOCVD of GaN, AlN, AlGaN, and InGaN films has resulted in the demonstration of high-quality epilayers and, for the case of GaN, net donor concentrations as low as $n \sim 10^{15}$ cm^{-3} for unintentionally doped films grown on sapphire. Furthermore, high-conductivity p-type Mg-doped GaN MOCVD-grown films have also been demonstrated. This will be useful for the growth of N-P-N HBT's in the InAlGaN system.

In this program, we will grow high-quality epilayers and heterostructure electronic devices using the wide-bandgap binary compounds AlN, GaN, and InN, the ternary compounds $Al_xGa_{1-x}N$, $In_xAl_{1-x}N$, and $In_xGa_{1-x}N$, and the quaternary compound $In_x(Al_yGa_{1-y})_{1-x}N$. We will perform growth of films in the InAlGaN alloy system using commercially available high-purity precursors. Specifically, triethylgallium (TEGa) will be employed as the Ga source and a compatible Al source, triethylaluminum (TEAl) or trimethylaluminum (TMAl), which have been shown to be capable of producing high-quality AlGaAs, will be used as the Al precursor. In addition, we will also evaluate triethylaminealane (TEAA) as a source for Al. Trimethylindium (TMIn) will be used as the In source, since it is a solid with a fairly high vapor pressure. In the initial phase of our studies, we have used NH_3 as a source of N but we will evaluate other options, e.g., tertiarybutylamine. The use of TEGa and NH_3 for the growth of high-quality epitaxial GaN films has already been established in Dupuis' group at UT-Austin. We also have developed Mg p-type doping in InAlGaP materials and p-type doping experiments will soon be undertaken in the nitrides. Post-growth annealing studies, similar to those we have already performed in InAlGaP, will be carried out to determine the optimum thermal cycle to reduce the atomic H passivation of the Mg acceptors in our films. The use of Si and Sn dopants for producing controlled n-type carrier concentrations in the nitrides will also benefit from our extensive experience with these dopants in InAlGaP and AlGaAs materials growth studies.

The choice of the appropriate substrate for epitaxy of these films is a critical issue. Up to this time, most GaN, AlN, and AlGaN films have been grown on (0001) sapphire substrates. In this program, we will explore MOCVD growth of III-V nitride films on both sapphire and SiC substrates. For power device applications, a high-conductivity SiC substrate is preferred because the device must carry a large current through the backside contact. The SiC substrate is also preferred because of its high thermal conductivity.

The sources employed in a majority of the recent MOCVD studies are NH_3 and conventional organometallic precursors, e.g., trimethylgallium (TMGa) and trimethylaluminum (TMAl). While some promising results have recently been obtained, fundamental problems related to dislocations, defects, and stoichiometry control remain to be solved. To reduce these problems, we will investigate novel low-temperature buffer layers for the growth of hetero-epilayers in this material system. Specially designed buffer layer structures will be employed to reduce the strain and dislocation density in the epilayers. Lattice-matched epitaxial structures will be grown and the effects of controlled strain and lattice-mismatch will be studied.

An important feature of this program is the growth and characterization of lattice-matched ternary and quaternary films and heterostructures in the InAlGaN system. Strained-layer superlattice (SLS) buffer layers will be employed to reduce the strain and dislocation density in epilayers. Fundamental studies of the optical, electrical, and structural properties of these materials will also be performed. This information will be important in establishing processing technologies for power switching devices in the InAlGaN system.

7.4.2 MOCVD of SiC/III-V Heterojunctions

Purdue has taken delivery of an Aixtron MOCVD system capable of growing GaN, AlN, GaAlN, and SiC. With this capability, J. M. Woodall and M. R. Melloch will investigate the heterojunction properties of all-epilayer SiC/III-V structures, in contrast to previous work done on heterostructures in which the III-V nitride epilayers were deposited on SiC substrates. This is important for several reasons. First, the all-epilayer structures will demonstrate the fundamental advantages and limitations of this system both electronically and structurally. Second, the AlN/SiC system may provide an alternate route for high quality MOSFET power switching devices. Lastly, SiC may become the preferred substrate for all III-V nitride devices, including power devices. It is well known in the case of III-V arsenides and phosphides that the ability to grow epitaxial buffer layers of the substrate material prior to the in-situ deposition of related materials generally results in devices with improved performance. Therefore, the ability to grow SiC buffer layers in-situ on SiC substrates followed by in-situ III-V nitride epitaxial growth is likely to produce similar benefits.

7.4.3 MBE of III-V Nitrides

Growth of GaN and AlGaN by MBE will be done at UT-Austin by B. G. Streetman and his group in a new system designed specifically for these materials, employing a novel plasma-enhanced nitrogen-cracking source developed in our laboratory. As mentioned above, the source uses an RF plasma to obtain a beam of atomic nitrogen from a N_2 stream in a He carrier gas. The purpose of the He is threefold—to enhance the plasma, to increase the velocity of the N through the outlet orifice, and to provide shielding between atomic N atoms in the stream. Using this N source and a standard Ga metal effusion cell, we have grown GaN on sapphire substrates with growth rates approaching those of "standard" III-V MBE (about 0.6 μm/hr). This is an important breakthrough, since MBE growth of GaN using standard ECR sources of N has resulted in growth rates closer to 0.2 μm/hr. Therefore, the use of MBE for nitride growth becomes much more practical with this source, and the outstanding capabilities of MBE for accurate layer-by-layer growth will become available to study interesting new devices employing nitrides. This new source will be installed in a recently purchased EPI growth chamber, which is compatible with our other two Varian Gen II chambers used for arsenides and phosphides. Streetman's group has an established history of productive research in the growth of multilayer heterostructures by MBE and the application of the resulting layers in a broad range of electronic and optoelectronic devices. The work supported here will be leveraged by Prof. Streetman's research in the NSF Science and Technology Center seeking to develop novel chemical precursors for nitride growth and to find convenient substrates having a better lattice match for GaN growth. We have already begun to study several spinels and perovskites which are promising candidates for lattice-matched growth of GaN.

7.4.4 MBE of P-type GaInP Layers for MOSFET Power Devices

The achievement by J. M. Woodall of p-type GaAs surfaces with low surface state densities which are long-term stable in air points the way to revisit GaInP as a material for MOSFET power switching applications. It has been theoretically predicted that GaInP MOSFET structures should exhibit a nearly 20-fold improvement over Si MOSFET structures for power switching applications. The problem is that up until now it has not been possible to fabricate good p-MOS capacitors using III-V arsenides and phosphides which can be driven into inversion. Therefore, as a subsidiary activity to the development of both SiC and III-V nitrides for power switching applications, we will attempt to fabricate p-GaInP structures with reduced surface states. If successful, we will then attempt to fabricate p-MOS capacitors with reduced interface traps. Pending success, this will be followed by the design and fabrication of a p-MOSFET structure for switching applications. This research will be limited in scope, and is meant to be a novel back-up approach to the main research on SiC and the nitrides.

7.4.5 Development of Fabrication Technology for the III-V Nitrides

Development of unit processes for device fabrication in the III-V nitrides is still incomplete. Recent work on reactive-ion etching (RIE) using $SiCl_4$ and CH_4 plasmas has shown some success, and UT-Austin will study this technique to evaluate selective etching capabilities of various gases. Wet chemical etching using conventional acids is very slow for GaN and AlN. The UT-Austin group has recently achieved some success using wet chemical etchants, and will explore this further.

UT-Austin and Purdue will investigate refractory metals for high-temperature-compatible ohmic and Schottky contacts to the III-V nitrides. Ti-Al and Au-Sn have been used for ohmic contacts in Hall samples on the nitrides, and Ti-Pt-Au should be applicable as well. We will also investigate Ti-Pt-based contacts for high-temperature operation, and we will explore the formation of Schottky barriers using pure Au. Ohmic-contact and Schottky-barrier technologies for the As- and P-based III-V semiconductors are well established at UT-Austin, and this knowledge will be exploited to develop contacts to the nitrides.

In addition, Purdue will investigate the doping of the nitrides via liquid phase diffusion. This will be done as a result of Prof. Woodall's expertise on both the thermochemical and electrochemical effects on diffusion coefficients and dopant site selection during diffusion and crystal growth. Lastly, Woodall will investigate the use of a new cermet, C-Si-O-metal, as a high temperature stable ohmic or Schottky barrier contact to both the nitrides and SiC. This material has already been demonstrated by Woodall as a useful Schottky barrier contact to p-type GaAs.

7.5 Device Design, Simulation, and Parameter Verification

The device design activity will be lead by T. Paul Chow of Rensselaer Polytechnic Institute. Prof. Chow has over fifteen years experience in the design and fabrication of silicon power devices, including MOSFET's, IGBT's, thyristors, and MCT's. Device simulation will be an important part of the design activity. A major problem with all available simulation programs is the inability to model anisotropic mobility. This is critical for SiC, where the electron mobility is highly anisotropic, varying by a factor of four in the 6H polytype. To support Prof. Chow's simulation activity, Prof. J. L. Gray of Purdue will modify his 2-D simulation program ADEPT to include both anisotropic mobility and non-isothermal internal conditions. This will give us a unique capability for accurate simulation of SiC power devices.

One of the challenges in designing devices for SiC and the III-V nitrides is the lack of accurate values for many of the fundamental parameters. A major portion of the design effort will be devoted to model parameter verification. This will be accomplished by comparing model predictions with experimental measurements on prototype devices. Purdue is compiling a database of SiC parameters from measurements made under the BMDO-sponsored NVRAM program. These parameters include surface generation velocity and minority carrier lifetime as a function of doping. Cree has extensive measurements on hole and electron mobility in both 4H and 6H-SiC. By combining these data, we can calculate hole and electron diffusion lengths in SiC, parameters which are essential for simulation of BJT's, IGBT's, and MCT's.

The first devices to be developed under the MURI program will be SiC power MOSFET's and power UMOSFET's. During the second and third years we will investigate SiC IGBT's and MCT's. During the third year, increasing emphasis will also be placed on devices in the III-V nitrides. **In all device design activities, special attention will be paid to techniques for edge termination and field suppression to increase breakdown voltage.**

One advantage of the III-V nitride family is the availability of heterojunctions, and we will take advantage of bandgap engineering to enhance device performance. Possible novel devices include the heterojunction bipolar transistor (HBT) and the heterojunction field-effect transistor (HFET). For example, it may be possible to use a GaN/AlN HFET to control the base current of a GaN BJT in a manner analogous to the silicon IGBT. This device might be called a "heterojunction gate bipolar transistor" (HGBT). We will investigate these and other novel device concepts in the III-V nitrides.

7.6 Device Fabrication and Characterization

SiC device fabrication will be conducted both at Purdue and Cree. Purdue and Cree have all the necessary equipment in place, as discussed in Section 4.2. The unit processes include selective-area doping by ion implantation, ion-implant activation, anisotropic etching by RIE, thermal oxidation, deposition of thick field and intermediate dielectric layers, ohmic and Schottky contact deposition and annealing, polysilicon deposition and doping, and metal interconnect deposition.

Device fabrication in the III-V nitrides will be conducted primarily at Purdue, but UT-Austin will fabricate test structures and prototype devices to provide feedback on material quality. At Purdue, Cooper and Melloch have extensive experience in III-V device fabrication. During the 1980's, they pioneered the development of one-transistor dynamic memory cells in GaAs. They also developed AlGaAs/GaAs depletion-load MODFET integrated circuits and fabricated a 42-transistor JFET dynamic content-addressable memory (DCAM) in GaAs. Both Purdue and UT-Austin have all the necessary equipment to fabricate power devices in the III V nitrides.

7.7 Tasks and Schedules

Our program to develop power switching devices in SiC and the III-V nitrides is organized into twelve major tasks. These tasks are listed in the table below, along with the sections in the proposal where they are described and the responsible investigators. Approximate schedules for each task are shown in Fig. 12. We caution that in a research program of this type it is impossible to predict with absolute certainty when any particular phase of the investigation will be completed, and error bars grow larger as we move further into the program.

	Section	Task Description	Investigator(s)	Instit.
1	7.3.1	SiC crystal growth and materials improvement	Carter	Cree
2	7.3.1	Study of defects limiting minority carrier lifetime in SiC (to make bipolar power devices feasible)	Cooper, Melloch Carter, Palmour	Purdue Cree
3	7.3.2	Wide-area growth of SiC on silicon wafers	Spencer	Howard
4	7.3.3	Substrate bonding to attach SiC wafers to a silicon wafer for processing on silicon production lines	Melloch, Cooper Himelick	Purdue Delco
5	7.3.4	Adaptive manufacturing for yield enhancement	Cooper, Melloch	Purdue
6	4.2 & 7.3.5	Optimization of the SiO_2/SiC MOS interface and study of oxide reliability	Cooper, Melloch	Purdue
7a	7.4.1	MOCVD of III-V nitrides	Dupuis Carter	Texas Cree
7b	7.4.2	MOCVD of SiC/III-V nitride heterojunctions	Spencer Melloch, Woodall	Howard Purdue
8	7.4.3	MBE of III-V nitrides	Streetman	Texas
9	7.4.5	Development of unit processes for device fabrication in the III-V nitrides	Woodall, Melloch Dupuis	Purdue Texas
10	7.5	Device design, simulation, and parameter verification for SiC and III-V power devices	Chow Palmour Cooper, Melloch	RPI Cree Purdue
11	4.2 & 7.6	SiC device fabrication and characterization	Cooper, Melloch Palmour	Purdue Cree
12	7.6	III-V device fabrication and characterization	Cooper, Melloch Dupuis	Purdue Texas

Table 2. Major tasks and responsible investigators in this MURI program.

Scheduled Activity — Activity which will depend on results of earlier research

Task	Task Description	Institution
1	Optimize SiC crystal growth to increase wafer size & reduce defects	Cree (funded by ARPA)
2	Study defects limiting minority carrier lifetime in SiC for bipolar devices	Purdue Cree
3	Growth of 3C-SiC on Si using compliant-layer techniques	Howard
4	Study feasibility of processing SiC/Si bonded wafers on Si line Develop substrate bonding of SiC wafers to silicon wafers	Purdue Delco
5	Apply adaptive manufacturing to prototype power devices	Purdue
6	MOS optimization (Si-face) MOS optimization (a-axis) Study MOS oxide reliability	Purdue
7a	MOCVD of III-V nitrides	Texas, Cree
7b	MOCVD of SiC/III-V heterojunctions	Howard, Purdue
8	MBE of III-V nitrides	Texas (Streetman)
9	Develop unit processes for III-V nitride fabrication	Purdue Texas
10	Design & simulate SiC MOSFET's Design SiC thyristors, MCT's, & IGBT's Design and simulate III-V nitride power devices (HBT's and HFET's)	RPI, Cree, Purdue
11	Fabricate SiC MOSFET's (Prototype) (Full Size) Fabricate SiC thyristors and/or IGBT's (Prototype) (Full Size)	Purdue Cree
12	Fabricate III-N power devices	Purdue Texas

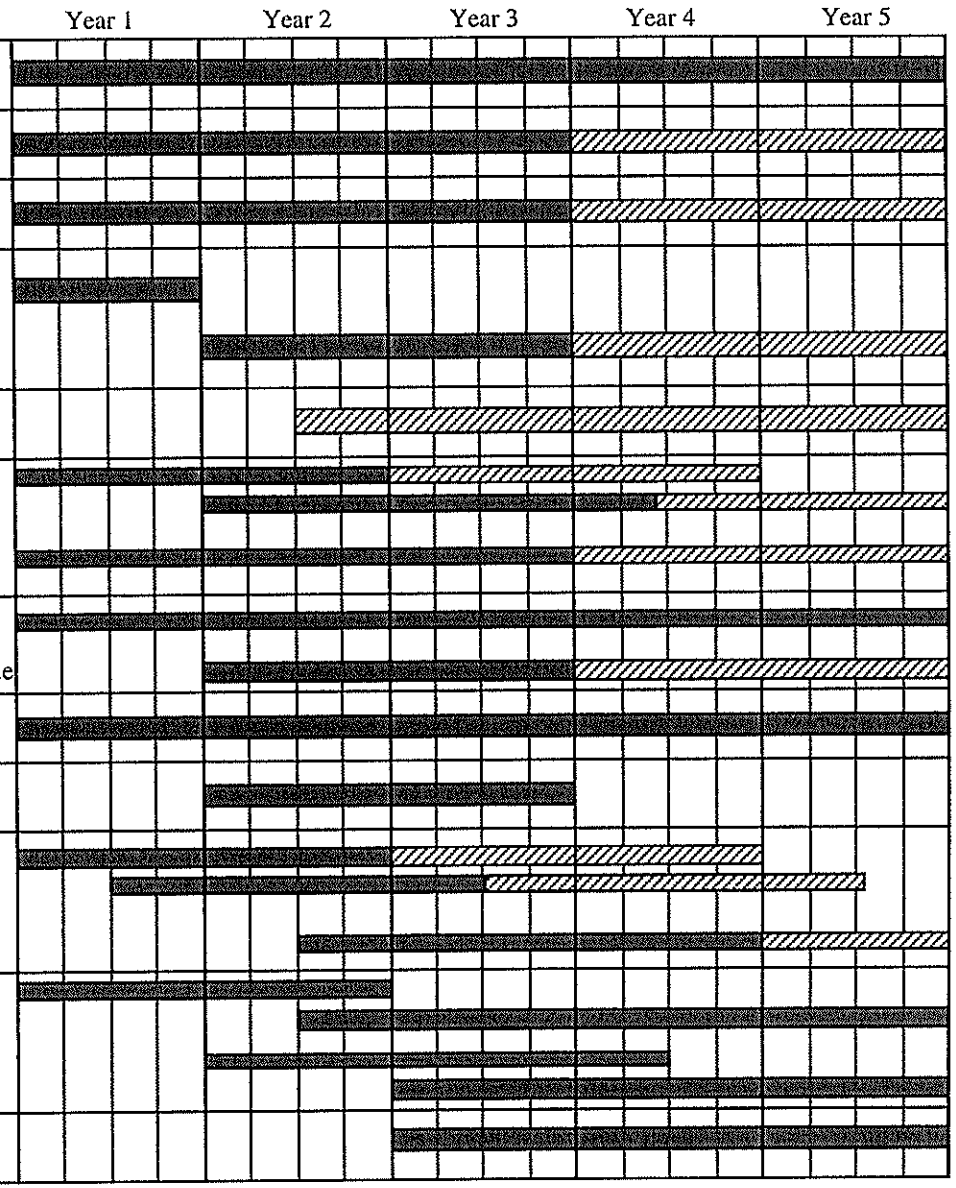


Figure 12. Time sequence for major tasks in this proposal.

8. Qualifications of Key Investigators

Calvin H. Carter, Jr., Vice President, New Product Development at Cree Research, has over 15 years of experience in research related to silicon carbide, and is also a co-founder of Cree Research. He has been co-Principal Investigator or Program Manager on all of Cree's funded research contracts (totaling >$19M) and was co-PI on two funded Office of Naval Research grants on silicon carbide while at North Carolina State University. Dr. Carter has extensive experience in SiC crystal growth, thin film deposition, doping, and material characterization and developed the first commercially viable SiC boule growth process. Since joining Cree, he has increased the diameter of SiC bulk crystals from 10 mm to 50 mm, increased crystal thickness by 560% and improved the crystal quality by orders of magnitude. Much of the recent progress was made possible by a $2M NIST Advanced Technology Program on which he was co-PI. He was also co-PI on a $2.4M ARPA contract which demonstrated the first SiC/AlGaN single crystal alloy, increased the brightness of SiC blue LEDs from 17 μW to 35 μW. He is Program Manager on another ARPA funded program which will soon lead to the release of a much brighter blue LED based on GaN grown on SiC substrates. Dr. Carter was responsible for establishing a closed-stock company affiliate in St. Petersburg, Russia (Cree Research-Eastern European Division) and has recruited 3 of the premier Russian SiC scientists to work for Cree in the US. In addition to the ONR funded programs at NCSU, Dr. Carter was co-PI on a National Science Foundation sponsored grant on diffusion in SiC as well as other grants related to SiC for structural applications. He was also co-PI and program manager on an SDIO funded program on the growth and characterization of GaN and AlN on SiC substrates. Dr. Carter is co-inventor on 7 issued U.S. patents, 2 pending U.S. patent applications, and 1 issued foreign patent and has 57 publications on SiC and other electronic materials.

T. Paul Chow received his B.A. degree in mathematics and physics (summa cum laude) from Augustana College, Sioux Falls, S. Dakota, in 1975, M.S. degree in Materials Science from Columbia University, New York City, New York, in 1977 and Ph.D. degree in electrical engineering from Rensselaer Polytechnic Institute, Troy, New York, in 1982. His doctoral thesis was a process-related study of refractory metals and metal silicides for VLSI MOS applications. From 1977-1989, he worked at General Electric Corporate Research and Development, Schenectady, NY. In the first two years, he was involved with developing CVD processes and characterization of doped tin oxide and indium oxide thin films for transparent electrode applications in solid-state imagers. From 1979-1982, his work on refractory metals and metal silicides included the deposition and plasma etching of these films as well as their incorporation into integrated-circuit processes and performance characterization of test devices and logic circuits. From 1982 to 1989, he participated in the design and process development of various discrete and integrable MOS-gated unipolar and bipolar devices (such as the MOSFET, IGBT and MCT). Also, he was involved with process architecture and integration of high-voltage integrated circuits. Since 1989, he has been in the faculty of the Electrical, Systems and Computer Engineering Department of Rensselaer Polytechnic Institute, Troy, NY, as an Associate Professor. His present research interests are in developing new device concepts and circuit models for high-voltage power devices and integrated circuits, process integration of ULSI metallization, and in process research of silicon and wide bandgap compound semiconductors. Dr. Chow has published over 40 papers in refereed scientific journals, presented over 70 conference talks, contributed 3 chapters in technical textbooks and has over 10 patents. He received the Solid State Science and Technology Young Author Award of the Electrochemical Society in 1982 and the Horizon Award from Augustana College in 1986. He is a member of the Electrochemical Society and IEEE. He is also presently the Associate Editor for Solid State Power for the IEEE Transactions on Electron Devices.

James A. Cooper, Jr. received his Ph.D. degree from Purdue University in 1973. In his thesis research he expanded the bias regime of the MOS conductance technique, the most powerful method for characterizing the MOS interface, and his work is cited in the authoritative MOS text

by Nicollian and Brews. In 1973 he joined the technical staff of Bell Laboratories, Murray Hill, NJ. While at Bell Labs, he served as principal designer of the WE-8000, AT&T's first CMOS microprocessor, and with D. F. Nelson developed a time-of-flight technique for measuring the high-field drift velocity of electrons in inversion layers on silicon. In 1983 he became Professor of Electrical Engineering at Purdue University, where he was founding Director of the Purdue Optoelectronics Research Center. From 1983 - 1991 his research centered on novel devices in GaAs. During this time, he fabricated and characterized a contiguous-domain millimeter-wave oscillator in GaAs, a device he co-invented with K. K. Thornber of Bell Labs. Along with M. R. Melloch, he developed the first one-transistor dynamic RAM cells in GaAs. His students also fabricated GaAs MODFET integrated circuits and demonstrated a 42-transistor dynamic content addressable memory using JFET technology in GaAs. Between 1986 and 1991, Cooper and Melloch increased the storage time of GaAs memory cells from 30 sec to over 10 hours, equivalent to an order of magnitude improvement every two years. In 1990 he and Melloch began to investigate nonvolatile RAM cells in SiC in collaboration with J. W. Palmour and C. H. Carter of Cree Research. During this time they fabricated the first vertically-integrated bipolar NVRAM cell in SiC, the first CCD's in SiC, and the first monolithic digital integrated circuits in SiC. Prof. Cooper is a Fellow of the IEEE and served as Associate Editor of IEEE Transactions on Electron Devices from 1983 through 1986. He has co-authored over 110 technical papers and conference presentations, 3 book chapters, and holds 8 US patents (with two others pending).

Russell D. Dupuis is Professor of Electrical and Computer Engineering at the University of Texas at Austin and holds the Judson S. Swearingen Regents Chair in Engineering. He received his BSEE in 1970 from the University of Illinois at Urbana-Champaign with Highest Honors (Bronze Tablet). Dupuis earned his MSEE, and PhDEE degrees in 1971 and 1973, respectively also from the University of Illinois at Urbana-Champaign. In 1973, he joined the Semiconductor Research and Development Laboratory of Texas Instruments where he studied the liquid-phase epitaxial growth of GaP:N and GaP:ZnO for green and red light-emitting diodes (LED's). In 1975 he joined the Electronics Research Center of Rockwell International where he was the first to show that MOCVD could be used in the growth of high-quality semiconductor thin films and he was the first to demonstrate the growth of AlGaAs-GaAs injection lasers by any vapor-phase epitaxial process. Dupuis was also the first to grow high-quality AlGaAs-GaAs quantum-well heterostructures by MOCVD and the first to demonstrate room-temperature CW operation of AlGaAs-GaAs quantum-well injection lasers grown by any materials technology and the first to establish that such lasers can be reliable enough for practical use. In 1979, Dupuis joined the Materials Science Research Department of the Solid State Electronics Research Laboratory of AT&T Bell Laboratories where he continued his research on AlGaAs-GaAs lasers grown by MOCVD as well as studied the growth of InP-InGaAsP lasers and photodetectors by the MOCVD process. He was the first to grow InP-InGaAsP lasers by atmospheric-pressure MOCVD and the first to grow InP-InGaAs avalanche photodetectors by this process. His most recent work involves the MOCVD growth of heteroepitaxial AlGaAs-GaAs and InGaAsP-InP lasers on Si substrates, vertical-cavity surface-emitting lasers in the InGaAs-InP system, and high-speed InGaAs-InP heterojunction bipolar transistors (HBT's). Prof. Dupuis joined The University of Texas at Austin in September of 1989. He is a Professor in the Microelectronics Research Center where he has established a research group to study novel approaches to the MOCVD materials technology and MOCVD growth of advanced semiconductor device structures. Dupuis has received several honors and awards for his work, including: the National Academy of Engineering (1989); Distinguished Alumnus Award, Dept. of Elect. & Computer Eng., University of Illinois (1987); Young Scientist Award of the Gallium Arsenide and Related Compounds Conference (1986); Fellow of the Institute of Electrical and Electronics Engineers (1987); Distinguished Member of the Technical Staff, AT&T Bell Laboratories (1986); IEEE Morris N. Liebmann Field Award (1985). He has published over 140 technical articles in reviewed archival journals and has given many invited talks, including invited lectures in the Soviet Union.

Michael R. Melloch: In August 1984 Prof. Melloch joined the School of Electrical Engineering at Purdue University as an Assistant Professor and is presently a Full Professor and Assistant Dean of Engineering there. At Purdue University he developed a III-V MBE facility and a SiC/III-V Nitride CVD facility. Record efficiency GaAs solar cells have been fabricated from material produced in this MBE facility. Dr. Melloch's group at Purdue University did some of the early work on characterizing sulfide surface treatments of GaAs and in collaboration with Dr. Eli Yablonovitch, then at Bell Communications Research, demonstrated a permanent As_2S_3 passivation of a GaAs heterojunction bipolar transistor. Dr. Melloch's group was the first to investigate the effects of bandgap narrowing in GaAs (due to heavy impurity doping) on the electrical performance of devices. They were also the first to characterize both the electron and hole minority carrier mobilities in GaAs as a function of majority carrier concentration using a zero-field time-of-flight technique. In 1990, in collaboration with Nobuo Otsuka, Dr. Melloch discovered As clusters in GaAs epilayers that were grown at low substrate temperatures by MBE and subsequently annealed. In collaboration with Jerry Woodall and Nobuo Otsuka, he has reduced to practice the formation of these composite materials consisting of semimetallic As clusters in a GaAs semiconductor matrix. In collaboration with Prof. Cooper, Dr. Melloch has been involved with development of a nonvolatile memory cell in 6H-SiC; the development of the first digital circuits and CCD's in SiC; characterization of SiC MOSFET's and BJT's; and the characterization and improvement of the SiO_2/SiC interface. Currently, Dr. Melloch is engaged in research related to MBE of III-V materials; device structures utilizing metal-semiconductor composites; SiC material characterization and devices; and CVD of SiC and the III-V nitrides. He has co-authored over 150 technical papers, over 190 conference presentations, 2 book chapters, and 3 patents.

John W. Palmour, Senior Scientist at Cree Research, is the person primarily responsible for the development of 6H-SiC and 4H-SiC power MOSFETs for high temperature use at Cree. He is also responsible for the development of high voltage, high temperature SiC thyristors and for developing planar 6H-SiC MOSFETs, both n-channel and p-channel. Since joining Cree Research, as a co-founder of the company, Dr. Palmour has been co-PI on research contracts totaling >$14M. He has modeled, designed, and successfully fabricated 6H-SiC bipolar junction transistors, MESFETs, and JFETs for high temperature operation. Additionally, he has developed MESFETs and JFETs for high frequency and high power operation, and was the first to demonstrate the operation of SiC in the GHz frequencies. He has also fabricated differential pair MESFETs and MOSFETs, gigaohm resistors and SiC Schottky diodes for high temperature operation, developed device designs for several other types of SiC devices, and continued research on oxidation, dry etching, contacts and other aspects of processing SiC. Dr. Palmour is also responsible for the development of SiC-based nonvolatile random access memory at Cree in the joint program with Purdue University. Dr. Palmour's graduate work included extensive characterization of oxidation and reactive ion etching of 3C-SiC. Electrical contact and MOS capacitor development and characterization were also part of his graduate research. Dr. Palmour is also Chairman of Cree's Intellectual Property Committee and is the New Technology Representative for Cree's government sponsored programs. He is co-inventor on 8 issued U.S. patents, 6 pending U.S. patents and 4 issued foreign patents and has 69 publications related to silicon carbide.

Michael G. Spencer is Professor of Electrical Engineering and Director of the Materials Science Research Center of Excellence at Howard University. Dr. Spencer has over fourteen years of research experience in the epitaxial growth of compound semiconductors with recent emphasis on wide bandgap materials. Dr. Spencer is a recipient of the Presidential Young Investigator Award for 1985, the Alan Berman Research Publication Award from the Naval Research Laboratories in 1986, the White House Initiative Faculty Award for Excellence in 1988, a Distinguished Visiting Scientist appointment at Jet Propulsion Laboratories in 1989, and a NASA Certificate of Recognition in 1992. He received his BS and MS degrees in Electrical Engineering and his Ph.D. from Cornell University in 1981. Dr. Spencer's experience includes

two years at AT&T Bell Laboratories, where he supervised and managed the design, prototype production, and manufacture of two different product lines of power rectifiers. Dr. Spencer has authored over 50 publications in the area of compound semiconductor research, and has two patents pending.

Ben G. Streetman is Professor of Electrical and Computer Engineering and Director of the Microelectronics Research Center at The University of Texas at Austin and holds the Dula D. Cockrell Centennial Chair in Engineering. His teaching and research interests include semiconductor materials and devices, growth of multilayer heterostructures by molecular beam epitaxy, radiation damage and ion implantation, luminescence, and advanced lasers and detectors for optoelectronic devices. After receiving the Ph.D. from The University of Texas at Austin (1966), he was on the faculty (1966-1982) of the University of Illinois at Urbana-Champaign. He returned to UT-Austin in 1982. In 1989 he received the Education Medal of the Institute of Electrical and Electronics Engineers (IEEE). In 1987, he was elected to membership in the National Academy of Engineering and in the same year received the AT&T Foundation Award of the American Society for Engineering Education (ASEE). In 1981 he received the Frederick Emmons Terman Award of the ASEE. In 1980 he was elected Fellow of the IEEE, and in 1990 was chosen as one of the twelve first Fellows of the Electrochemical Society. He has served on numerous committees and panels, including the NAS/NAE/IoM Government-University-Industry Research Roundtable Council. He serves on the Science and Technology Advisory Council for ALCOA, and for many years served on the Research Advisory Committee for United Technologies. He is the author of the book *Solid State Electronic Devices* (Prentice- Hall, 1972, 1980, 1990, 1995), which has been translated into Japanese, Korean, and Polish. He has published more than 240 articles in the technical literature. Twenty-nine students of Electrical Engineering, Materials Science, and Physics have received their Ph.D.'s under his direction.

Jerry M. Woodall, the Charles William Harrison Distinquished Professor of Microelectronics at Purdue University, received a B.S. in metallurgy in 1960 from MIT. In 1982, he was awarded a Ph.D. in Electrical Engineering from Cornell University. Early in his career, he pioneered the horizontal Bridgman growth of both high purity and highly perfect GaAs crystals, and the fabrication of SiC p-n junctions using both Al diffusion and the traveling solvent method. He then pioneered the development of the liquid phase epitaxial (LPE) growth of Si doped GaAs IR high efficiency LEDs used today in remote control applications such as TV sets. This was followed by seminal work on the LPE growth of GaAlAs and GaAlAs/GaAs heterojunctions used in super-bright red LEDs and lasers used, for example, in CD players and short link optical fiber communications. His present work involves the MBE growth of III-V materials and devices with special emphasis on metal contacts and doping studies. His efforts are recorded in over 200 publications in the open literature, 62 issued U.S. patents, and 10 patent applications filed. His accomplishments have been recognized by five major IBM Research Division Awards, 30 IBM Invention Achievement Awards, the 1980 Electronics Division Award of the Electrochemical Society, the 1984 IEEE Jack A. Morton Award, the 1985 Solid State Science and Technology Award of the Electrochemical Society, the 1988 Heinrich Welker Gold Medal and the International GaAs Symposium Award, his election as Fellow of the American Physical Society in 1982, his election as IBM Fellow in 1985, his election as President of the Electrochemical Society in May of 1990, his election to the National Academy of Engineering in 1989; his election to: IEEE Fellow in 1990, Electrochemical Society Fellow in 1992, and American Vacuum Society Fellow in 1994; the 1990 Medard Welch (Founders) Award from the American Vacuum Society, and an $80,000 IBM Corporate Award in 1992 for the invention of the GaAlAs/GaAs heterojunction.

9. Facilities

Purdue University, RPI, Howard University, UT-Austin, and Cree Research have all the equipment necessary to conduct the proposed research. A list of the major pieces of equipment at the university laboratories is given below:

Purdue University: Tempress furnace tubes for SiC wet/dry oxidation and LPCVD polysilicon deposition, two Varian GEN-II MBE systems for III-V material growth (one system consists of two independent growth chambers connected by vacuum transfer tube), Aixtron AIX 200/4 MOCVD system for SiC and III-V nitride epilayer growth, Varian E-beam evaporator, Airco E-beam evaporator, two NRC thermal evaporators, Perkin-Elmer 3140 sputtering system, Perkin-Elmer 240 magnetron sputtering system, MRC 8620 sputtering system, Technics PD-II PECVD deposition system , Accelerators, Inc. AM-210 (200 kV) ion implanter, AG Associates Mini-Pulse RTA system, Lindberg 1700 °C tube furnace, Cambridge EBMF-2.5 direct-write-on-wafer E-beam exposure machine, Gyrex 1005 optical pattern generator, Electro-Mask 10:1 step and repeat system, three Karl Suss MJB-3 optical mask aligners, Millitron ion milling machine, Technics PE-II plasma etching system, Dry-Tek plasma etching system, Dry-Tek RIE system, Plasma Technology Plasmalab RIE system, Polaron DLTS system, Kiethley integrated Hi-Lo CV measurement system, HP 4274A and 4275A LCR meters, HP 4140B picoammeter, HP 7145A parameter analyzer, Blue-M convection oven (300 – 977 K), two Micromanipulator probe stations with heated chucks (300 – 673 K).

Rensselaer Polytechnic: IBM RS-6000 workstations for device design, simulation, and layout, Sony-Tektronix 370A curve tracer with high voltage switching circuit (1000 V), 500 MHz digitizing oscilloscope, microcomputer-based CV and IV measurement system, probe station with high-temperature chuck, DLTS system.

Howard University will use an epitaxial reactor with two chambers, one dedicated to III-V nitrides and alloys and the other to SiC. The chambers are vacuum interlocked, and films of either nitrides or carbides can be grown without breaking vacuum. Howard also has a full complement of fabrication equipment, including ion implantation, MBE, deep-UV mask aligners, E-beam and thermal evaporators, plasma etching, ion milling, and characterization equipment including scanning Auger microprobe, TEM, RBS, DLTS, PL and CL.

UT-Austin: Emcore GS3200 MOCVD reactor, JEOL Model 6400 SEM, BioRad Model 4300 electrochemical profiler, Blake Industries five-crystal X-ray diffractometer, Rigaku 2.0 kW X-ray generator, Karl Suss MJB-3UV lithography system, Guardian Systems gas scrubber, Turbo-pumped four-hearth E-beam metal evaporator, RIE system, Ti-sapphire tunable tripled femtosecond laser, EPI system for growth of nitrides, with proprietary PE source of atomic N.

10. Plans for Student Training

A major goal of this MURI program will be to train graduate students in material science and device research in the wide bandgap semiconductors. We will transfer technology to US companies through joint collaborative projects with industry, summer internships, and eventual graduation and permanent placement of graduate students. Some examples are given below.

Under the MURI program, Profs. Melloch and Cooper of Purdue and Dr. James Himelick of Delco Electronics (Kokomo, IN) will jointly supervise one or two MS students who will study the feasibility of processing SiC wafers on existing silicon production lines. Dr. Himelick will receive an adjunct appointment at Purdue University for the purposes of this supervision.

In 1994 Purdue was awarded a contract for SiC power device development by the Semiconductor Research Corporation (SRC). Under the SRC program, Dr. C. E. Weitzel of Motorola PCRL serves as an industrial mentor to Purdue. SRC encourages student internships,

and during the summer of 1994, Scott Sheppard, a graduate student from the Purdue group, spent a summer internship with the Motorola SiC group. This internship was considered successful by both groups, and Motorola and Purdue plan to continue summer internships and other forms of mutual collaboration under the MURI program.

Howard University, as a historically black institution, plays a unique role in educating minority graduate students, particularly black Americans. This MURI program will make it possible for Howard to support and train many more minority students in the materials sciences, thereby enhancing minority representation in science and engineering in this country.

11. Summary of the Proposal

SiC device technology is sufficiently mature that commercial production of power devices can be anticipated in the next 3 – 5 years. Although it offers many advantages, SiC is very different from silicon, and power device concepts cannot be directly translated from silicon to SiC. It is essential that this project be conducted by researchers with experience in SiC materials issues, SiC device design, and SiC fabrication technology. Purdue and Cree have the necessary SiC experience. Purdue is the world leader in optimizing the MOS interface on SiC, an interface which is crucial for both power MOSFET's and for bipolar devices such as the IGBT and MCT. Purdue also has fabricated some of the most sophisticated SiC devices, including the first monolithic digital integrated circuits in SiC, the first SiC CCD's, and the first one-transistor nonvolatile memories. Cree Research is the world leader in SiC power device fabrication, having demonstrated the best SiC bipolar transistors, the best SiC thyristors, the best planar SiC MOSFET's, and the first (and only) vertical power UMOSFET's in SiC.

Our program includes a direct path to take SiC and/or III-V nitride power device technology from research to development to manufacture. This path is made possible through the participation of Cree Research as a full partner in this program. Purdue and Cree have collaborated on SiC device development since 1990, and are currently participating in a $4.2M BMDO-funded joint program to develop SiC nonvolatile RAM technology. Cree will soon begin a $6.9M research program, supported by ARPA and internal funds, to increase SiC wafer size and reduce defect density. Cree has also made a corporate decision to develop a line of SiC (and/or III-V nitride) power switching devices for commercial manufacture. By aligning the MURI program on power device development with (a) the Purdue/Cree BMDO program on SiC fabrication technology, (b) the Cree ARPA program on materials improvement, and (c) Cree's internal commitment to power device production, the overall impact of the MURI program will be significantly leveraged and enhanced.

The III-V nitrides GaN and AlGaN show great potential for high-performance power devices of the future, but several important materials issues need to be addressed before these devices can be commercialized. The main difficulty arises from the lack of a suitable lattice-matched substrate for GaN crystal growth. We will address these materials issues in this program. R. D. Dupuis of UT-Austin is currently growing the highest quality GaN ever reported by any growth technique on any substrate. We will build on his success and attempt to take his results still further. In parallel activities, B. G. Streetman will investigate novel MBE techniques for growth of the nitrides, and M. G. Spencer will explore the growth of GaN on large-area substrates by compliant-layer techniques. Cree Research will act as a third source of device-quality III-V nitride epilayers and heterojunctions. If device development is successful, Cree Research will manufacture and market III-V nitride power devices grown on SiC substrates.

It is important for national defense purposes as well as for national competitiveness that US companies take a leadership position in these emerging fields. Our proposal is designed to enhance the position of US companies relative to the rapidly growing activities of their European and Japanese competitors. This will be accomplished through technical exchanges and student internships with Motorola PCRL, through a joint feasibility study of high-volume production with Delco Electronics, and through the participation of Cree Research as a full partner in this project.

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13. Cost Proposal

A detailed budget follows. Below is a discussion of the travel and capital funds requested, and of the cost sharing.

The travel funds in the budget will be used to attend scientific meetings for the purpose of presenting the developments of this program and keeping abreast of developments in the areas of power devices and silicon carbide/III-V nitride materials. Travel funds will also be used to attend any program reviews and for any necessary meetings between the subcontractors and Purdue.

The University of Texas at Austin is budgeting for three items of capital equipment in the first year. The first items are mass flow controllers required for modifications of the existing MOCVD system to provide for the installation of additional dopant sources. The second item is a vacuum pump required for additional pumping speed because of the high flow rates of ammonia and hydrogen. The third item is a dewar required for variable-temperature Hall effect measurements and variable-temperature photoluminescence studies.

Howard University requests capital funds in the first year for an atomic force microscope (AFM). The AFM will be used to analyze the nature of the surface right after initiating growth.

Rensselaer Polytechnic Institute is requesting capital funds for two items. In the first year RPI will purchase a parametric analyzer, which will be used for static characterization of devices such as pn diodes and bipolar junction transistors. In the second year RPI will purchase a pulse generator, capacitance-voltage meter, and a personal computer to enable dynamic switching of power devices and capacitance-voltage measurements of MOS structures and Schottky diodes. The computer will allow interfacing of the various pieces of equipment for data acquisition.

Purdue University requests capital equipment funds in the second year of this program for the purchase of an LCR meter for MOS interface characterization and a vacuum annealing furnace for ohmic contact annealing.

Purdue University will provide $50,000 per year ($250,000 during the five years of the MURI) in cost sharing. Rensselaer Polytechnic Institute will contribute an amount equal to approximately 20% of their budget in the form of cost sharing. This amounts to about $40,000 per year for five years. Cree Research will provide cost sharing in the form of a 1:1 match of up to $100,000 per year ($500,000 during the five years of the MURI) for the purchase of material by the other members of this program. In addition, Cree will provide cost sharing in the form of a 1:1 match of $33,075 per year ($165,375 during the five years of the MURI) for the material that Cree uses in the pursuit of this program.

The **total cost sharing** during the five years of the MURI program by Purdue, RPI, and Cree will be approximately **$1,121,321**.

3. THE INSTITUTION: Signature and typed name and address of university official authorized to obligate contractually, and with whom business negotions should be conducted.

(b) (6) [redacted]
(Signature)

7/10/95
(Date)

WILLIAM D. GRIGGS
(Title) (First Name) (MI) (Last Name)

(317) 494-6200
(Phone Number, including Area Code)

Purdue Research Foundation
Legal Name of Grantee (University)

Hovde Hall
Street Address (P.O. Box Numbers Cannot Be Accepted)

West Lafayette IN 47907
(City) (State) (Zip Code)

4. CERTIFICATIONS BY OTHER UNIVERSITY OFFICIALS: Use this space for names, titles, and signatures of other officials you wish to approve submission of this proposal (e.g., the Principal Investigator and Department Head, Dean or other officials). A separate sheet may be submitted if additional signatures are required. Recall that all sheets must render the entire proposal no more than 50 pages in length.

(b) (6) [redacted]
Principal Investigator (Typed name plus signature)
James A. Cooper, Jr.

7/7/95
Date

(b) (6) [redacted]
Other Official (Typed name plus signature)
D. A. Landgrebe, Acting Head, School of Electrical and Computer Engineering

7/7/95
Date

(b) (6) [redacted]
Richard J. Schwartz, Dean, Schools of Engineering

7/10/95
Date

TOTAL BUDGET

				8/95-7/96	8/96-7/97	8/97-7/98	Sub-Total	8/98-7/99	8/99-7/00	Sub-Total	TOTAL
A. Salaries and Wages											
1. Senior Personnel											
J. Cooper	AY	35%		(b) (4)							$210,640
	SS	2.0 mns									$110,024
M. Melloch	AY	25%									$118,012
	SS	1.5 mns									$72,695
J. Woodall	AY	10%									$67,990
	SS	1.5 mns									$104,703
J. Gray	AY	5%									$3,658
	SS	.5 mn									$3,805
2. Other Personnel											
P. Chin	FY	25%									$43,448
Grad Students	AY	50%	(10)								$646,709
	SS	3.0 mns	(10)								$197,892
Total Salaries & Wages				$313,916	$301,053	$313,094	$928,063	$319,370	$332,143	$651,513	$1,579,576
Grad fee remission				$23,110	$22,734	$24,876	$70,720	$27,234	$29,808	$57,042	$127,762
Total Compensation				$337,026	$323,787	$337,970	$998,783	$346,604	$361,951	$708,555	$1,707,338
B. Fringe Benefits											
Total fringe benefits				(b) (4)							$215,229
C. Total Compensation and Fringes				$379,814	$365,461	$381,313	$1,126,588	$389,544	$406,435	$795,979	$1,922,567
D. Non-Personnel direct costs											
Communications				$2,000	$2,080	$2,163	$6,243	$2,250	$2,340	$4,590	$10,833
Travel - Domestic				$11,000	$13,520	$14,061	$38,581	$14,623	$15,208	$29,831	$68,412
Travel - Foreign				$4,000	$0	$4,000	$8,000	$0	$0	$0	$8,000
Publication & Duplication				$6,000	$6,240	$6,490	$18,730	$6,749	$7,019	$13,768	$32,498
Supplies & Expenses				$73,462	$75,520	$79,301	$228,283	$81,451	$88,017	$169,468	$397,751
Scientific Equipment				$0	$67,668	$0	$67,668	$0	$0	$0	$67,668
SiC Purchases				$100,000	$100,000	$100,000	$300,000	$100,000	$65,000	$165,000	$465,000
Sub-Contracts											
University of Texas				$422,136	$416,284	$432,559	$1,270,979	$440,194	$457,783	$897,977	$2,168,956
Cree Research				$301,995	$312,669	$327,990	$942,654	$329,955	$330,696	$660,651	$1,603,305
RPI				$199,999	$200,001	$200,001	$600,001	$190,247	$189,839	$380,086	$980,087
Howard University				$249,948	$249,712	$249,647	$749,307	$239,948	$239,473	$479,421	$1,228,728
Total non-personnel direct costs				$1,370,540	$1,443,694	$1,416,212	$4,230,446	$1,405,417	$1,395,375	$2,800,792	$7,031,238
E. Total direct cost				$1,750,354	$1,809,155	$1,797,525	$5,357,034	$1,794,961	$1,801,810	$3,596,771	$8,953,805
F. Indirect cost (b) (4) of MTD cost				(b) (4)							$1,496,195
G. Total cost				$2,090,000	$2,090,000	$2,090,000	$6,270,000	$2,090,000	$2,090,000	$4,180,000	$10,450,000

Subcontract - University of Texas, Austin

	8/95-7/96	8/96-7/97	8/97-7/98	Sub-Total	8/98-7/99	8/99-7/00	Sub-Total	TOTAL
A. Salaries and Wages								
1. Senior Personnel								
Principle Investigators (partial summer salary)	$30,000	$31,600	$33,224	$94,824	$34,224	$35,873	$70,097	$164,921
2. Other Personnel								
Other Professionals								
Eng. Assoc. @ 1/3 time	$14,000	$14,560	$15,142	$43,702	$15,748	$16,378	$32,126	$75,828
Technician @ 1/3 time	$18,437	$19,000	$20,000	$57,437	$21,000	$22,000	$43,000	$100,437
Graduate Assistants (4)	$52,800	$56,256	$59,754	$168,810	$63,312	$66,900	$130,212	$299,022
Adminstrative Asst. @ 1/3 time	$11,000	$11,333	$12,000	$34,333	$13,000	$14,000	$27,000	$61,333
Total Salaries & Wages	$126,237	$132,749	$140,120	$399,106	$147,284	$155,151	$302,435	$701,541
Grad fee remission	$13,088	$13,265	$13,534	$39,887	$13,908	$14,286	$28,194	$68,081
Total Compensation	$139,325	$146,014	$153,654	$438,993	$161,192	$169,437	$330,629	$769,622
B. Fringe Benefits								
Total fringe benefits	(b) (4) [redacted]							$256,955
C. Total Compensation and Fringes	$185,731	$194,684	$204,954	$585,369	$215,066	$226,142	$441,208	$1,026,577
D. Non-Personnel direct costs								
Communications	$333	$333	$333	$999	$320	$403	$723	$1,722
Travel - Domestic	$6,600	$6,824	$7,057	$20,481	$7,056	$7,298	$14,354	$34,835
Publication & Duplication	$2,000	$2,040	$2,082	$6,122	$2,125	$2,170	$4,295	$10,417
Supplies & Expenses	$71,612	$77,171	$77,530	$226,313	$72,588	$73,001	$145,589	$371,902
Permanent Equipment	$28,000	$0	$0	$28,000	$0	$0	$0	$28,000
Total non-personnel direct costs	$108,545	$86,368	$87,002	$281,915	$82,089	$82,872	$164,961	$446,876
E. Total direct cost	$294,276	$281,052	$291,956	$867,284	$297,155	$309,014	$606,169	$1,473,453
F. Indirect cost (b) (4) f MTD cost	(b) (4) [redacted]							$695,503
G. Total cost	$422,136	$416,284	$432,559	$1,270,979	$440,194	$457,783	$897,977	$2,168,956

Subcontract - Cree Research Incorporated

Total Base Contract Cost: $1,061,724 Cost of Base to Government: $942,654 Cost of Option to Government: $680,564

		8/95-7/96	8/96-7/97	8/97-7/98	Sub-Total	8/98-7/99	8/99-7/00	Sub-Total	TOTAL
1. Clean Room Processing		$50,000	$50,000	$50,000	$150,000	$50,000	$50,000	$100,000	$250,000
2. Package & Test Department Costs									
Direct Labor	Hours	200	200	300		300	300		
Engineer ($31.15/hr)		$6,230	$6,479	$10,108	$22,817	$10,512	$10,932	$21,444	$44,261
	Hours	200	200	300		300	300		
P & T Technicians ($11.25/hr)		$2,250	$2,340	$3,650	$8,240	$3,796	$3,948	$7,744	$15,984
Total P & T Labor		$8,480	$8,819	$13,758	$31,057	$14,308	$14,880	$29,188	$60,245
P & T Fringes ([redacted] x Base)		$2,290	$2,381	$3,715	$8,386	$3,863	$4,018	$7,881	$16,267
P & T Overhead ([redacted] x Base)		$9,328	$9,701	$15,134	$34,163	$15,739	$16,368	$32,107	$66,270
Total P & T Department Costs		$20,098	$20,901	$32,607	$73,606	$33,910	$35,266	$69,176	$142,782
3. Mfg. Admin. Expenses = Total Direct Costs x[redacted]		$13,319	$13,471	$15,695	$42,485	$15,943	$16,201	$32,144	$74,629
Total Mrg. Direct Costs + Mfg. Overhead		$83,417	$84,372	$98,302	$266,091	$99,853	$101,467	$201,320	$467,411
4. R & D Department Costs									
R & D Labor	Hours	200	200	200		200	200		
PI - John W. Palm[redacted]									$51,044
PM - Calvin Carter[redacted]									$43,099
Device Scientist ($[redacted]									$182,260
Total R & D Labor		$53,170	$55,297	$57,509	$165,976	$54,131	$56,296	$110,427	$276,403
R & D Fringe & Occupancy ([redacted] Base)		$14,356	$14,930	$15,527	$44,813	$14,615	$15,200	$29,815	$74,628
R & D Overhead ([redacted] x Base)		$18,610	$19,354	$20,128	$58,092	$18,946	$19,704	$38,650	$96,742
Total R & D Department Costs		$86,136	$89,581	$93,164	$268,881	$87,692	$91,200	$178,892	$447,773

(b) (4)

Subcontract - Cree Research Incorporated

5. Services								
Ion Implantation	$4,400	$4,400	$4,400	$13,200	$4,400	$4,400	$8,800	$22,000
Poly Si Deposition	$9,000	$9,000	$9,000	$27,000	$9,000	$9,000	$18,000	$45,000
Deposited Oxide	$10,000	$10,000	$10,000	$30,000	$10,000	$10,000	$20,000	$50,000
Total Services	$23,400	$23,400	$23,400	$70,200	$23,400	$23,400	$46,800	$117,000
6. Supplies and Materials								
a. SiC Wafers w/ Epi (Catalog Pricing)	$79,380	$79,380	$79,380	$238,140	$79,380	$79,380	$158,760	$396,900
b. Photomasks	$10,000	$10,000	$10,000	$30,000	$10,000	$10,000	$20,000	$50,000
Total Supplies and Materials	$89,380	$89,380	$89,380	$268,140	$89,380	$89,380	$178,760	$446,900
7. Travel	$7,594	$12,254	$7,594	$27,442	$13,373	$8,742	$22,115	$49,557
Total Direct Cost and Overhead	$289,927	$298,987	$311,840	$900,754	$313,698	$314,189	$627,887	$1,528,641
8. G & A Expenses								
(b) (4) Total Direct Cost)	$46,388	$47,838	$49,894	$144,121	$50,192	$50,270	$100,462	$244,583
Subtotal	$336,315	$346,825	$361,735	$1,044,875	$363,890	$364,459	$728,349	$1,773,224
9. Facilities Capital Cost of Money	$5,370	$5,534	$5,946	$16,850	$5,755	$5,927	$11,682	$28,532
Total Cost	$341,685	$352,359	$367,680	$1,061,724	$369,645	$370,386	$740,031	$1,801,755
Less Cost Sharing	$39,690	$39,690	$39,690	$119,070	$39,690	$39,690	$79,380	$198,450
Cost to Government	$301,995	$312,669	$327,990	$942,654	$329,955	$330,696	$660,651	$1,603,305

Subcontract - Rensselaer Polytechnic Institute

	8/95-7/96	8/96-7/97	8/97-7/98	Sub-Total	8/98-7/99	8/99-7/00	Sub-Total	TOTAL
A. Salaries and Wages								
1. Personnel								
T. S. Chow AY 40%	(b) (4)							$135,616
SS 1.5 mns								$56,507
Graduate Research Assistant(s)								
AY 50%								$138,798
SS 3 mns								$89,832
Clerical Assistant								$10,577
Total Salaries & Wages	$81,235	$83,677	$86,196	$251,108	$88,777	$91,445	$180,222	$431,330
Grad fee remission	$32,400	$33,720	$35,040	$101,160	$36,420	$37,860	$74,280	$175,440
Total Compensation	$113,635	$117,397	$121,236	$352,268	$125,197	$129,305	$254,502	$606,770
B. Fringe Benefits (b) (4)	(b) (4)							$66,890
C. Total Compensation and Fringes	$126,234	$130,374	$134,603	$391,211	$138,964	$143,485	$282,449	$673,660
D. Non-Personnel direct costs								
Equipment	$25,000	$18,000	$0	$43,000	$0	$0	$0	$43,000
Travel - Domestic	$2,000	$2,060	$3,122	$7,182	$3,216	$3,312	$6,528	$13,710
Materials & Supplies	$6,774	$7,785	$14,770	$29,329	$10,865	$6,825	$17,690	$47,019
Publication Costs	$1,000	$1,030	$1,061	$3,091	$1,093	$1,126	$2,219	$5,310
Computer Services	$5,000	$5,150	$5,305	$15,455	$5,464	$5,628	$11,092	$26,547
Communications	$711	$560	$436	$1,707	$452	$466	$918	$2,625
Microfabrication Clean Room	$0	$0	$0	$0	$0	$0	$0	$0
Software License	$10,000	$10,300	$10,609	$30,909	$4,635	$4,700	$9,335	$40,244
Total non-personnel direct costs	$50,485	$44,885	$35,303	$130,673	$25,725	$22,057	$47,782	$178,455
E. Total direct cost	$176,719	$175,259	$169,906	$521,884	$164,689	$165,542	$330,231	$852,115
F. Indirect cost (b) (4) of MTD cost	(b) (4)							$333,920
G. Total cost	$239,594	$240,373	$241,165	$721,132	$232,231	$232,672	$464,903	$1,186,035
H. Cost Sharing								
10% AY in-kind of Chow Salary	$13,165	$13,561	$13,967	$40,693	$14,385	$14,816	$29,201	$69,894
ECSE Dept. 1/2 student tuition (in-kind)	$6,480	$6,744	$7,008	$20,232	$7,284	$7,572	$14,856	$35,088
3% AY Chow Salary	$3,950	$4,067	$4,189	$12,206	$4,315	$4,445	$8,760	$20,966
School of Engineering	$8,000	$8,000	$8,000	$24,000	$8,000	$8,000	$16,000	$40,000
Dean of Faculty	$8,000	$8,000	$8,000	$24,000	$8,000	$8,000	$16,000	$40,000
Total Cost Sharing	$39,595	$40,372	$41,164	$121,131	$41,984	$42,833	$84,817	$205,948
I. Total Funds Requested	$199,999	$200,001	$200,001	$600,001	$190,247	$189,839	$380,086	$980,087

Subcontract - Howard University

	8/95-7/96	8/96-7/97	8/97-7/98	Sub-Total	8/98-7/99	8/99-7/00	Sub-Total	TOTAL
A. Salaries and Wages								
1. Personnel								
Michael G. Spencer	(b) (4)							$78,535
Summer								
Xiao Tang								$67,911
1/4 Time								
Kobchat Wongchotigul								$40,621
1/4 Time								
Post Doc								$106,000
Total Salaries & Wages	$32,500	$62,900	$64,355	$159,755	$65,869	$67,443	$133,312	$293,067
B. Fringe Benefits	(b) (4)							
(b) (4) S & W)								$71,508
C. Total Compensation and Fringes	$40,430	$78,248	$80,058	$198,735	$81,941	$83,899	$165,840	$364,575
D. Non-Personnel direct costs								
Supplies	$14,200	$26,000	$24,000	$64,200	$20,009	$17,884	$37,893	$102,093
Publication Costs	$650	$1,000	$1,000	$2,650	$1,000	$1,000	$2,000	$4,650
Travel	$2,530	$2,950	$3,100	$8,580	$2,250	$2,250	$4,500	$13,080
Analytical Services (Univ of MD)	$37,250	$45,000	$45,000	$127,250	$42,008	$41,883	$83,891	$211,141
Equipment	$95,000	$0	$0	$95,000	$0	$0	$0	$95,000
Total non-personnel direct costs	$149,630	$74,950	$73,100	$297,680	$65,267	$63,017	$128,284	$425,964
E. Total direct cost	$190,060	$153,198	$153,158	$496,415	$147,208	$146,916	$294,124	$790,539
F. Indirect cost (b) (4) of MTD cost	(b) (4)							$438,189
G. Total cost	$249,948	$249,712	$249,647	$749,307	$239,948	$239,473	$479,421	$1,228,728

Delco Electronics

Subsidiary of
GM Hughes Electronics

February 28, 1995

Dr. James A. Cooper, Jr.
Professor of Electrical Engineering
Purdue University
1285 Electrical Engineering Building
West Lafayette, IN 47907-1285

Dear Jim:

As I have related in our telephone conversations, I am very interested in the silicon carbide development activities you and your students are pursuing. I feel that as a high temperature material, there are many applications in the automotive electronics environment for devices and circuits that can take advantage of the unique properties silicon carbide has to offer. To be sure, there is a great deal of research and development that needs to be done before we can realize a manufacturable process at low cost. But to that end, if there is anything I can do to assist in your research, I would be more than willing to help.

I am prepared to serve as a mentor and collaborator on this project, offering inputs on manufacturing constraints that might impede the rapid development of this technology. Our Advanced Development facilities (20,000 sq ft class 10 cleanroom) may be used to verify feasibility of process design. If we have any particular test or measurement equipment that can be of assistance in the evaluation of your devices and concepts, we would be happy to make them available. In addition, we are in the process of securing some supplemental funding that could be used in the support of a masters student. The approval process should be completed within one month. There are several other projects vying for these resources, but I feel confident that the area of high temperature materials development is one that will be recognized as a worthy candidate. Even if that funding is not approved, we will support your work as I have outlined above. Thank you for including Delco Electronics in your proposal.

Sincerely,

(b) (4)

James M. Himelick
Staff Development Engineer

Delco Electronics
Corporation
One Corporate Center
Kokomo, Indiana
46904-9005

MOTOROLA INC.

Phoenix Corporate Research Laboratories

February 28, 1995

Prof. J. A. Cooper
School of Electrical Engineering
Purdue University
West Lafayette, IN 47907-1285

Dear Prof. Cooper:

Subject: MURI Proposal "Manufacturable Power Switches"

Having read your "white paper" I was glad to hear that your team had been selected to submit a proposal to the Multidisciplinary University Research Initiative for "Manufacturable Power Switching Devices." Motorola is increasing its participation in the power semiconductor device market and therefore welcomes university programs that will help develop new technology and will train engineers for this important, emerging commercial market.

I support your emphasis on SiC devices with some moneys for III-V nitride devices which are several years behind. The ubiquity of silicon technology is based on understanding and controlling the Si / SiO_2 interface. I believe SiO_2 will play a similarly important role in the development of SiC technology. Your excellent work on developing an understanding of the SiO_2 / SiC interface gives your team a head start in this important area. The balance of your team is well positioned to cover the other important areas: SiC substrate size and quality, modeling and simulation, power device development, and III - nitrides.

Our previous collaborations [SRC Mentor (#94-SJ-378) "Development of Fabrication Technology for Power Devices in Silicon Carbide" and having Ph.D. candidate Scott Sheppard from your group as a summer employee] have been very beneficial to our SiC program at Motorola. Therefore I look forward to a continuing good interaction and a smooth transfer of information coming from this new program.

Sincerely,

(b) (6) [redacted]

Dr. C. E. Weitzel Member Technical Staff
Motorola, Inc. MS-EL508
Phoenix Corporate Research Laboratories
2100 E. Elliot Rd., Tempe, Arizona 85284
(602) 413-5906 FAX (602) 413-5934

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